UGPCB ELECTRONICS CO., LIMITED

Training Series for Process Technology of UGPCB

UGPCB ELECTRONICS CO., LIMITED

PCB &HDI Manufacturing Process and Process Fundamentals

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I. Basic Concepts

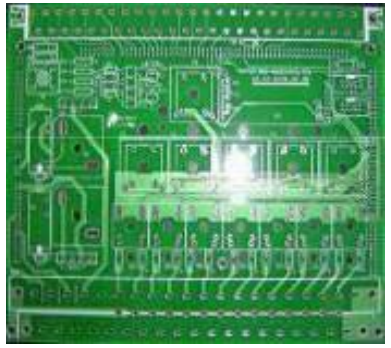
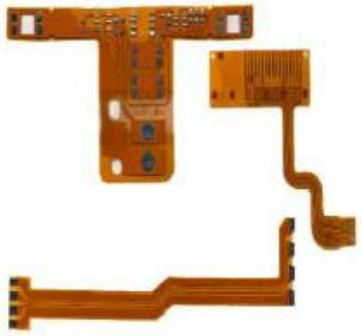
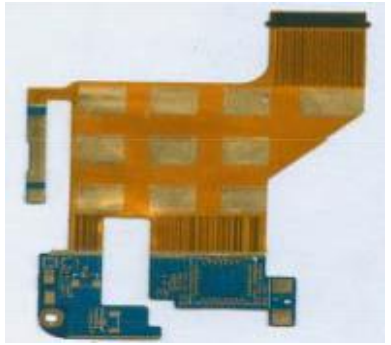
1.1 Definition of Printed Circuit Boards (PCBs)

A **printed circuit** refers to a conductive pattern formed on an insulating substrate by pre-designed printed circuits, printed components, or a combination of both. A **printed wiring** is a conductive pattern on an insulating substrate that provides electrical connections between components, excluding printed components.

The finished board of a printed circuit or printed wiring is called a **printed circuit board (PCB)** or **printed wiring board (PWB)**.

A **High Density Interconnection (HDI)** board is a high-end type of PCB, simply defined as a multi-layer board manufactured using the build-up method and micro blind vias. It is produced by first creating a core board (with or without plated through-holes) using traditional methods, then adding build-up layers with fine lines and micro blind vias on both outer layers.

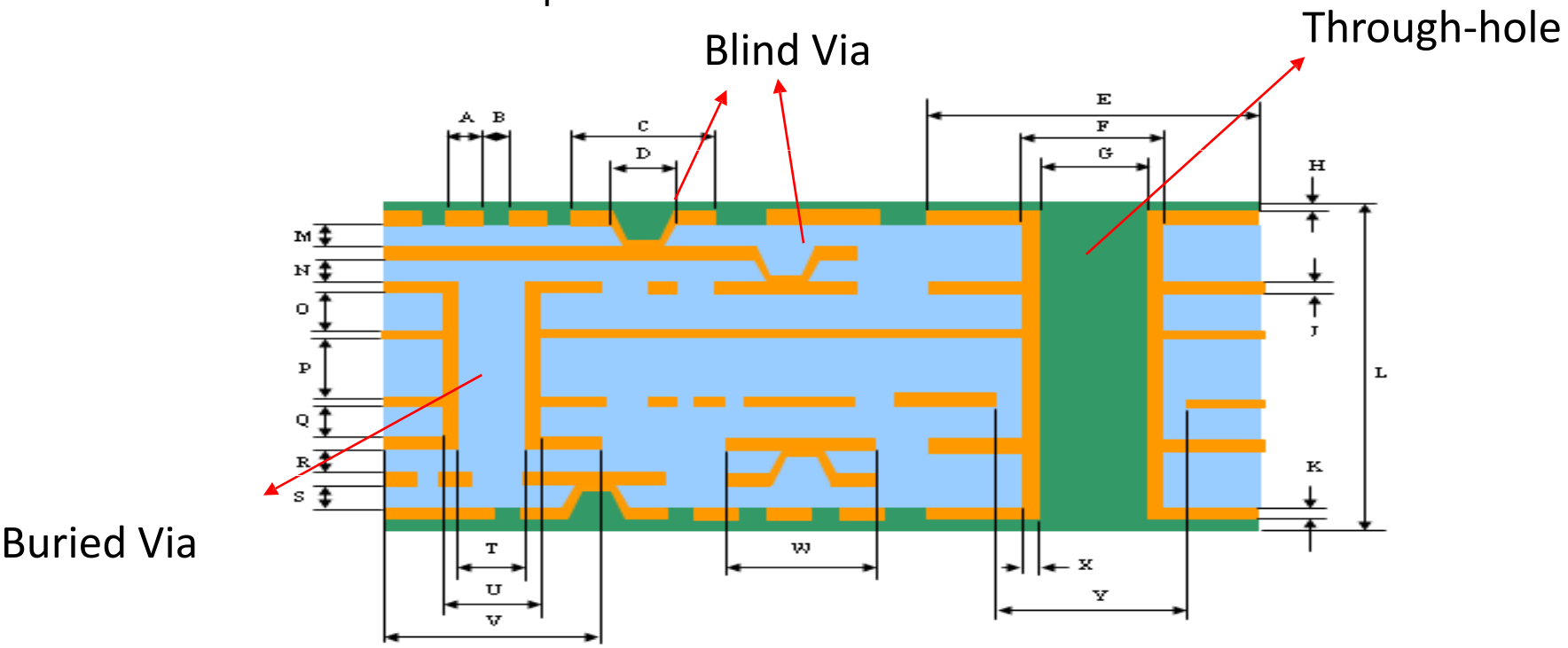
1.2 Classification of PCBs

No.	Classification Item	Types	Schematic Diagram
1	By Layers	Single-sided Board	 
		Double-sided Board	
		Multi-layer Board	
2	By Material	Rigid Board	 
		Flexible Board	
		Rigid-Flex Board	

Classification of PCB Vias

•Common via types: **Through-holes (NPTH/PTH)**, **Blind Vias**, **Buried Vias**

- PTH: Via holes and component insertion holes



1.4 Definition of HDI

HDI (High Density Interconnection) is a high-end type of PCB, typically defined as a circuit board with the following characteristics:

- Conductive layer thickness < 0.025mm
- Insulation layer thickness < 0.075mm
- Line width/line spacing ≤ 0.1/0.1mm
- Through-hole diameter ≤ 0.15mm
- I/O count > 300

It offers advantages of small size, high speed, and high frequency.

1.5 Applications of HDI Boards

Mainly used in mobile phones, cameras, camcorders, laptops, 3G data cards, portable electronic products, and other fields.



1.6 HDI Product Blind Via Types (1)

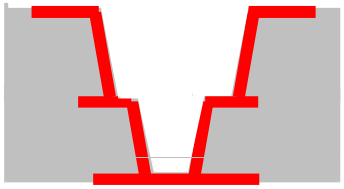
1st Order Blind Vias (Plus 1 Design)

An HDI board with 1 build-up layer added to one or both sides of a standard multi-layer board (n-layer board) is called a 1st Order HDI board (1+N+1 structure).

2nd Order Blind Vias (Plus 2 Design)

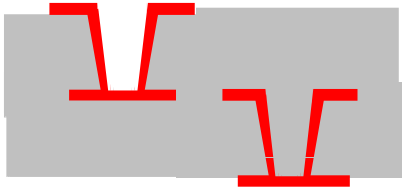
An HDI board with 2 build-up layers added to one or both sides of a standard multi-layer board (n-layer board) is called a 2nd Order HDI board (2+N+2 structure).

Stepped via



Skip via

Staggered via



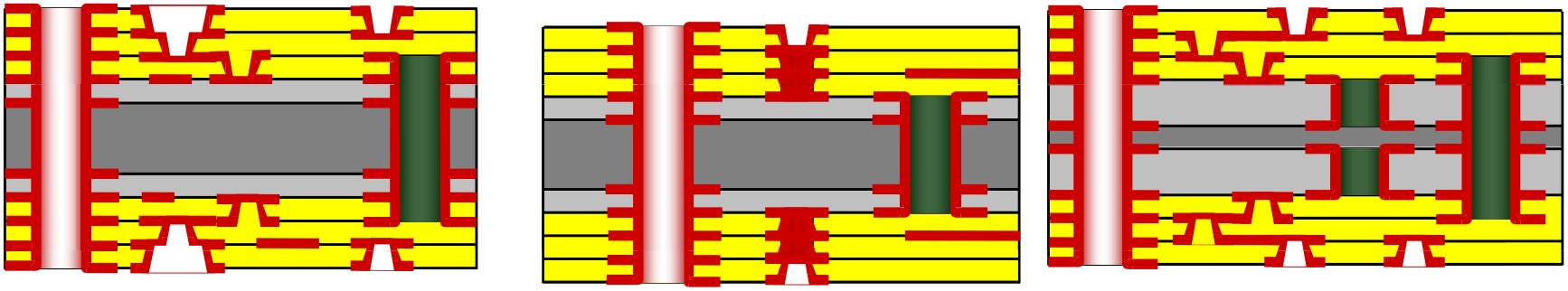
Stack via

I. Basic Concepts of HDI

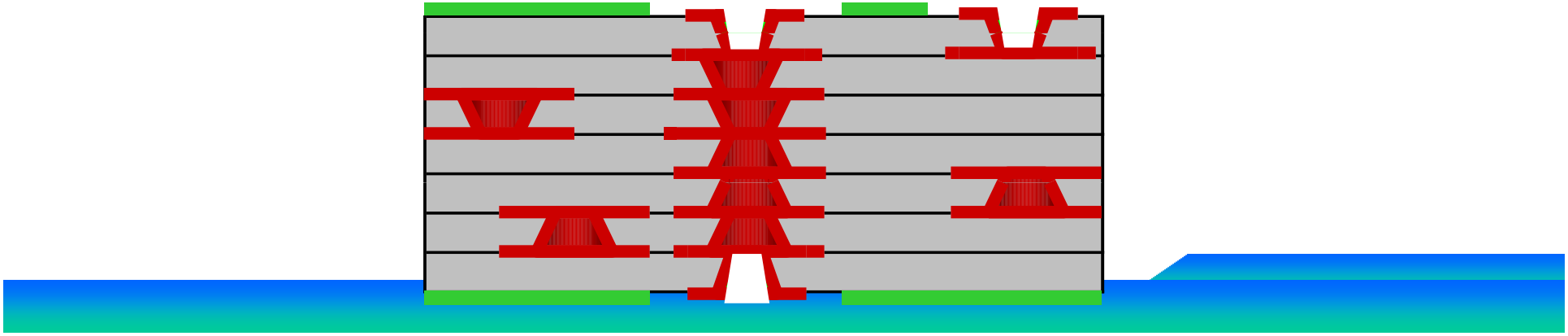
1.6 HDI Product Types (2)

High-order HDI: HDI boards with 3 or more build-up layers on one or both sides are called high-order HDI boards.

ELIC (Every Layer Interconnection): Also known as "Anylayer" PCB, it enables interconnection between any layers.



ELIC（Every Layer Interconnection）：（Anylayer）



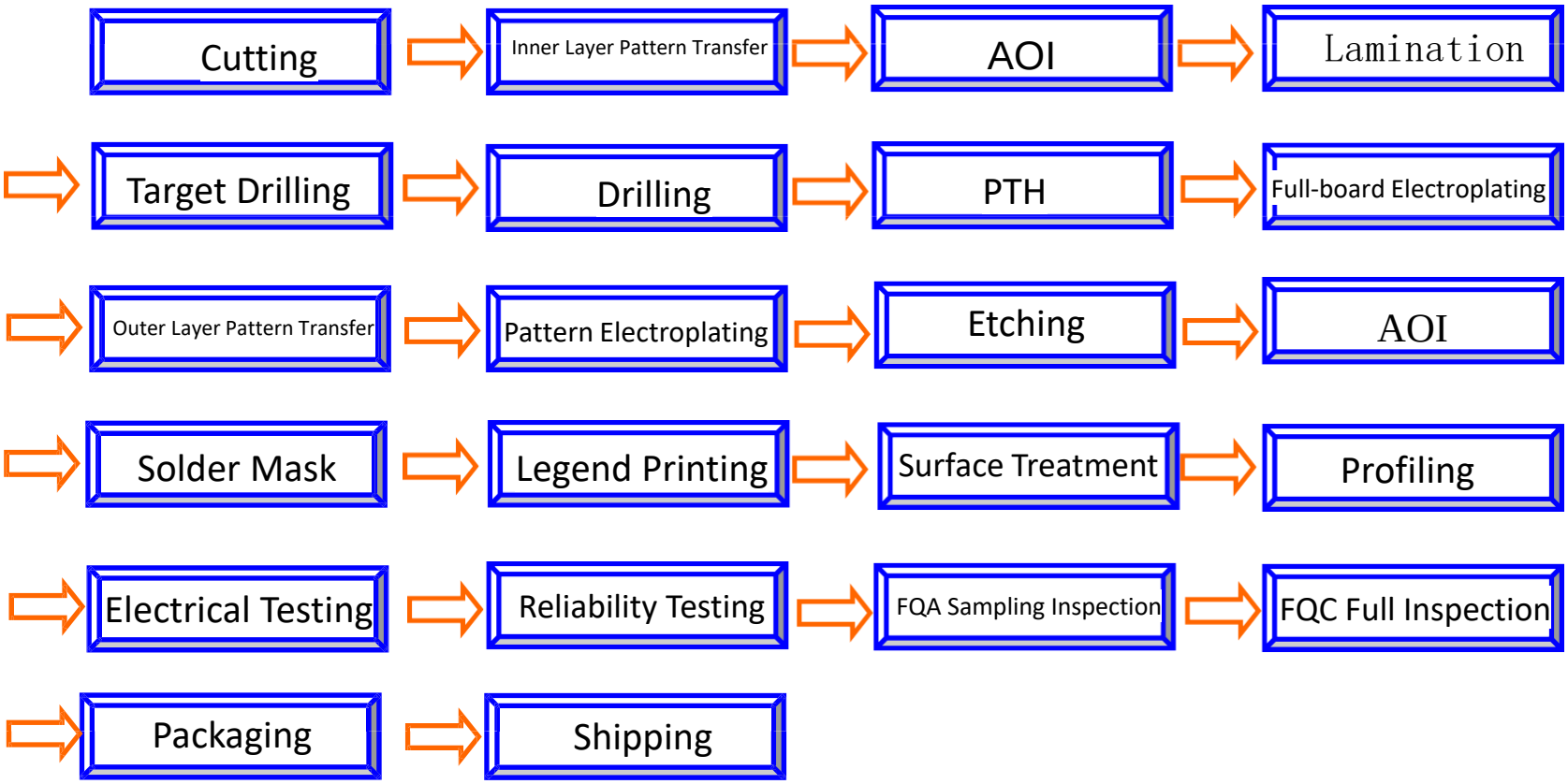
1.7 PCB Manufacturing Processes

Item	Process	Station	Main Function
1	Cutting	Board Cutting	Large CCL Sheets → Panels
2	Circuit Patterning	Inner 1, Inner 2... Outer Layers	Form circuit patterns
3	AOI	Automatic Optical Inspection(AOI/VRS)	Detect circuit defects (open circuits, short circuits, etc.)
4	Lamination	Lamination Station	Build-up layer formation
5	Drilling	Inner Drilling, Buried Drilling, Through Drilling	Drill through-holes
6	Electroplating	Buried Plating, General Plating, Filled-hole Plating, Plugging	Plate chemical copper on hole walls and surface
7	laser	Laser、DLD	Drill blind vias

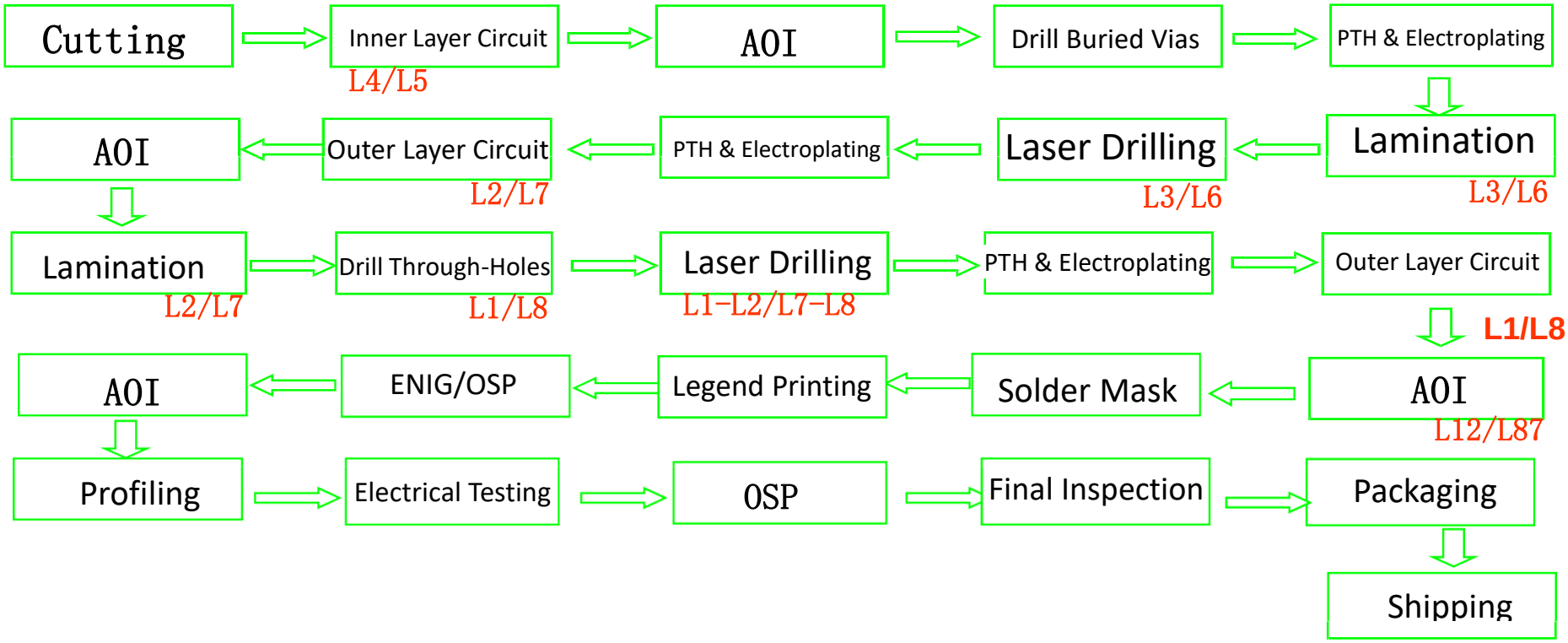
1.7 PCB Manufacturing Processes (Continued)

Item	Process	Station	Main Function
8	Solder Mask	Solder Mask, Legend Printing, ENIG Wet Film	Form solder mask layer and legend layer; replace partial ENIG dry film for selective ENIG
9	Surface Finishing	Full-board ENIG	Electroless Nickel Immersion Gold (ENIG)
10	Profiling	Routing, V-Grooving, Beveling	Panels → Sets (finished shape)
11	Surface Treatment	OSP, Immersion Tin, Immersion Silver	Protect copper surfaces
12	Electrical Testing	Electrical Testing, Via Inspection	Test electrical performance (open/short circuits) and check via diameter
13	FQC (Final Quality Check)	Visual Inspection, Warpage Check, Packaging	Inspect appearance, check board warpage, package products

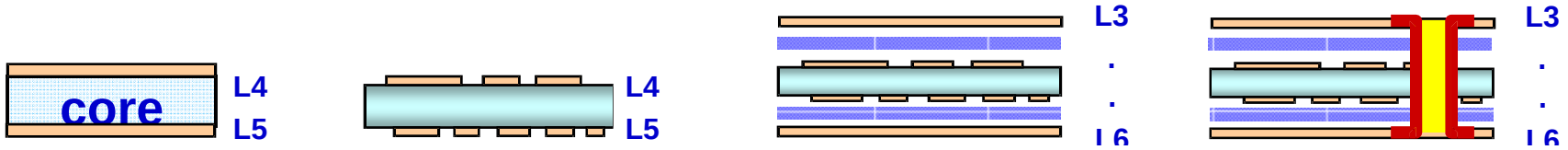
1.8 Standard Multi-layer PCB Manufacturing Flow



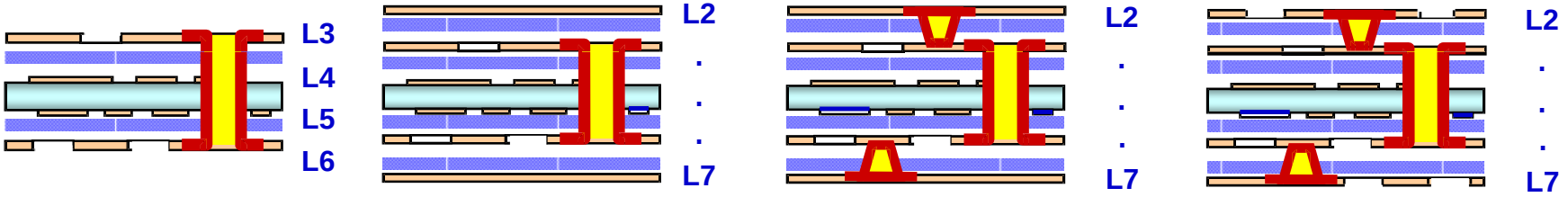
1.9 HDI Manufacturing Flow (8-Layer 2nd Order Board)



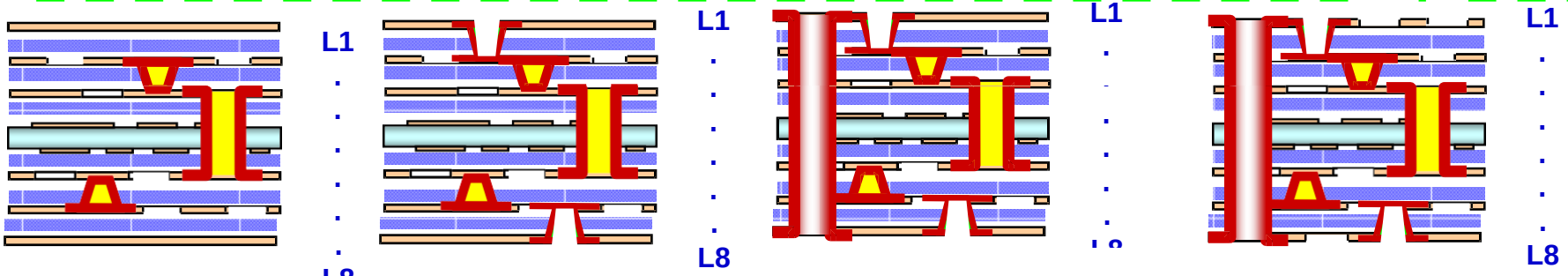
HDI Manufacturing Flow / Key Technology Diagram



CCL _ _ L4/L5Pattern Formation_ LaminationL3/L6 Drilling→PTH→Via Plugging

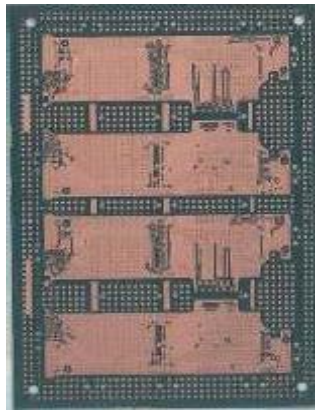


L3/L6 Pattern Formation LaminationL2/L7 Laser->Electroplating Pattern FormationL2/L7

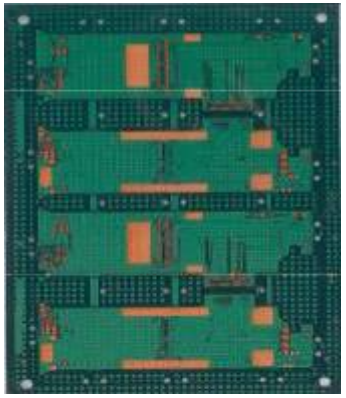


LaminationL1/L8 LASER Mechanical Drilling->Electroplating Pattern FormationL1/L8

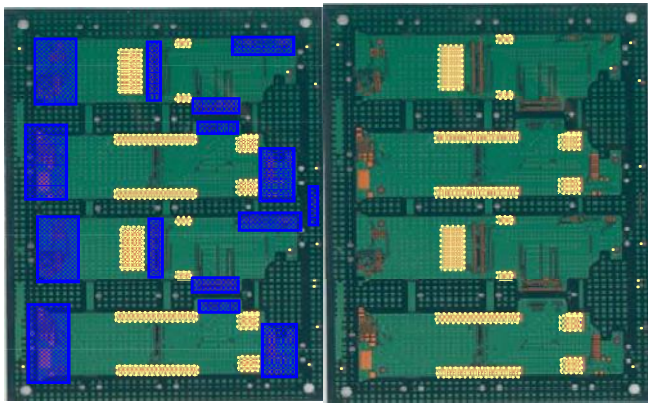
HDI Manufacturing Flow / Key Technology

→ 

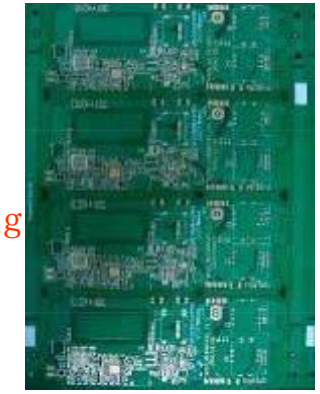
Outer Layer

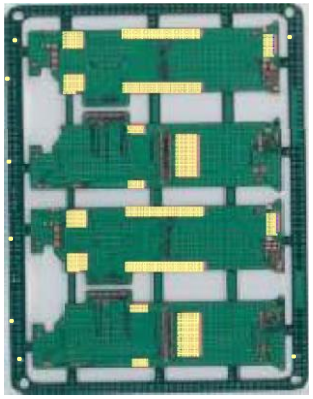


Solder Mask



Selective ENIG

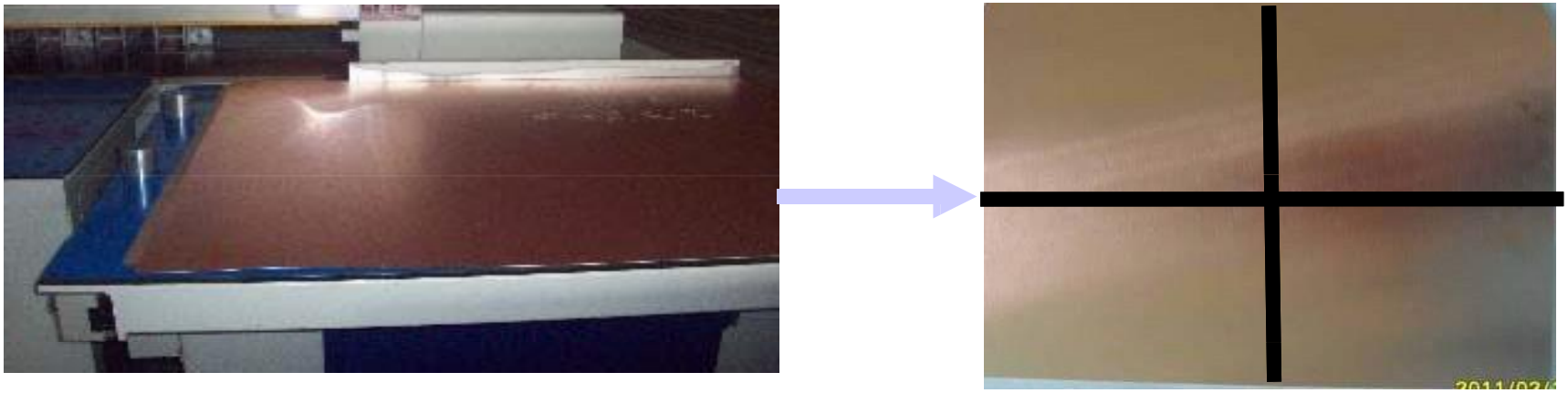
Legend Printing 

Profiling 

Electrical Testing→OSP→Final Inspection→Packaging→Shipping

II. Process Flow Introduction

1、Cutting



Cutting Principle	Cut large CCL sheets into working sizes according to pre-design dimensions
Main Materials	Copper Clad Laminate (CCL): Composed of copper foil and insulation layer, available in different board
	Composed of copper foil and insulation layer, available in different board thicknesses; copper thickness options include 1/3oz, 1/2oz, 1oz, 2oz, etc.

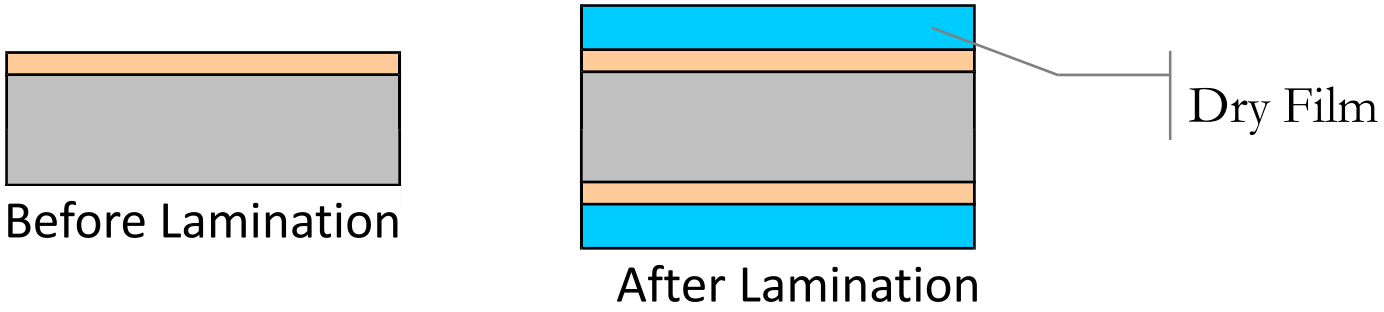
2、Inner Layer Fabrication Process

Flow: Cutting → Pretreatment → Dry Film Lamination → Exposure → DES (Development, Etching, Stripping)
Principle: Use image transfer to form inner layer circuits; "DES" is the abbreviation for integrated Development, Etching, and Stripping.

Inner Layer Process	Process Principle	Schematic Diagram
Pretreatment	Remove contaminants from copper surface; increase copper surface roughness via micro-etching to enhance adhesion between dry film and copper.	

Inner Layer Dry Film Lamination

Inner Layer Process	Process Principle	Schematic Diagram
Dry Film Lamination	Laminate dry film onto the pretreated copper surface using hot pressing rollers.	



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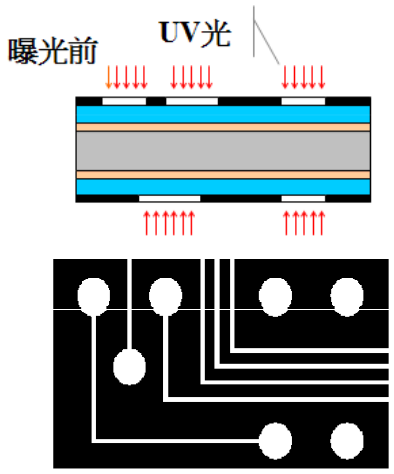
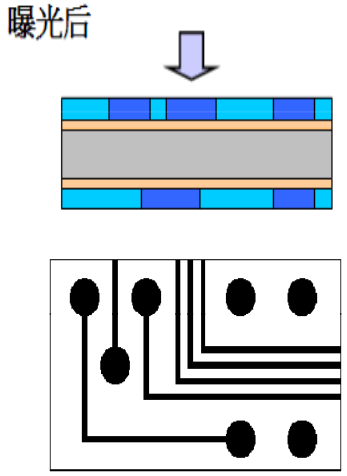
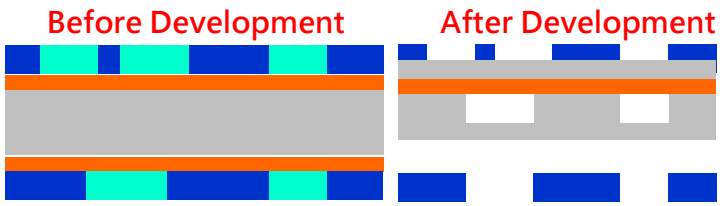
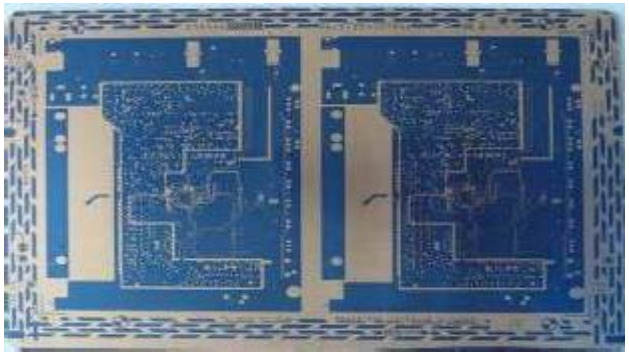
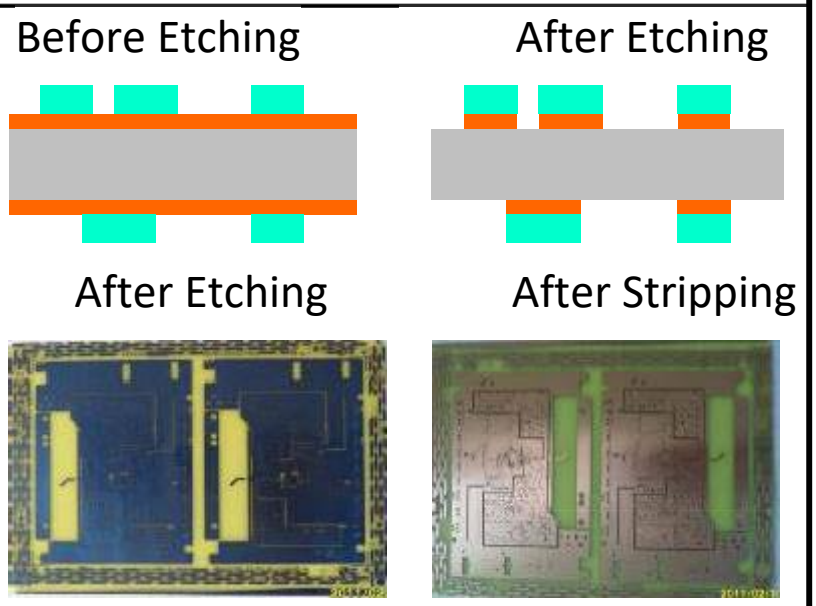
Inner Layer Exposure

Inner Layer Process	Process Principle	Schematic Diagram
Exposure	The dry film coated on the copper surface undergoes photo-curing reaction under light, transferring the pattern from the original film to the photosensitive substrate. - Negative Film: The required circuit pattern corresponds to the transparent (white) area of the film, which undergoes photo-polymerization; the opaque (black) area does not react. - Positive Film: Opposite to negative film; the required circuit pattern corresponds to the opaque (black) area of the film.	 Negative Film  Positive Film

Inner Layer Development

Inner Layer Process	Process Principle	Schematic Diagram
Development	Use alkaline solution to remove unpolymerized dry film/wet film; the polymerized dry film remains on the board as an anti-etching protective layer, revealing the required circuit pattern.	 

Inner Layer Etching

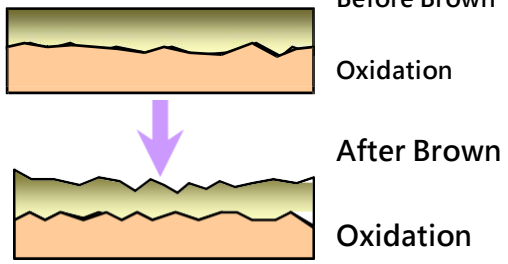
Inner Layer Etching	Process Principle	Schematic Diagram
Etching	Use etching solution to remove exposed copper after development, forming inner layer circuit patterns. Main Consumables: GC30 (main component: sodium chlorate), HCL, water.	

3. Lamination Process

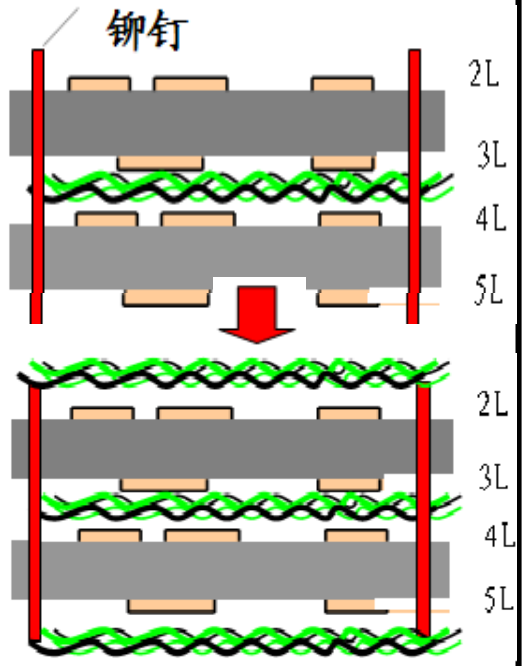
Flow: Brown Oxidation → Stacking → Riveting → Lamination → Post-treatment

Purpose: Laminate copper foil, Prepreg (PP), and roughened inner layer PCBs into multi-layer boards.

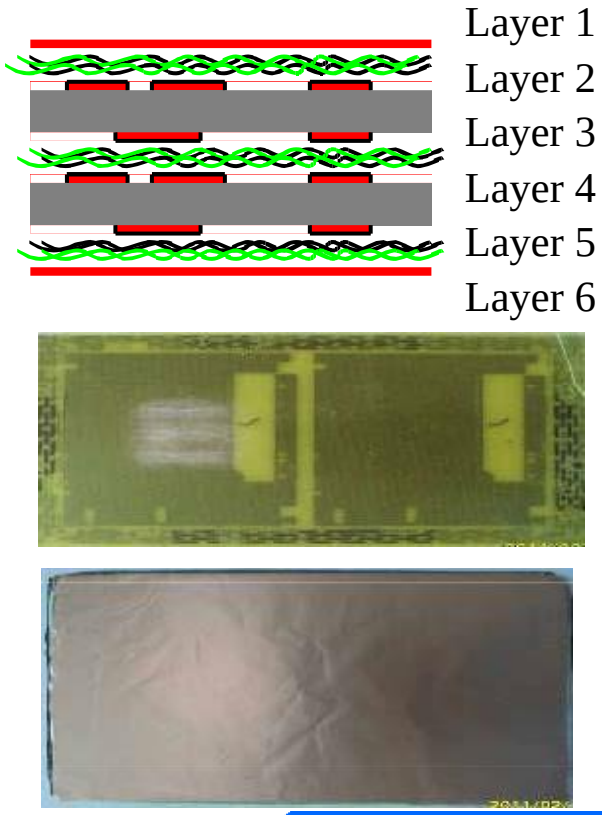
Brown Oxidation (for Lamination)

Lamination Process	Process Principle	Diagram (Before/After Brown Oxidation)
Brown Oxidation	Roughen copper surface via micro-etching to increase contact area between copper and resin, enhancing adhesion between prepreg and copper.	

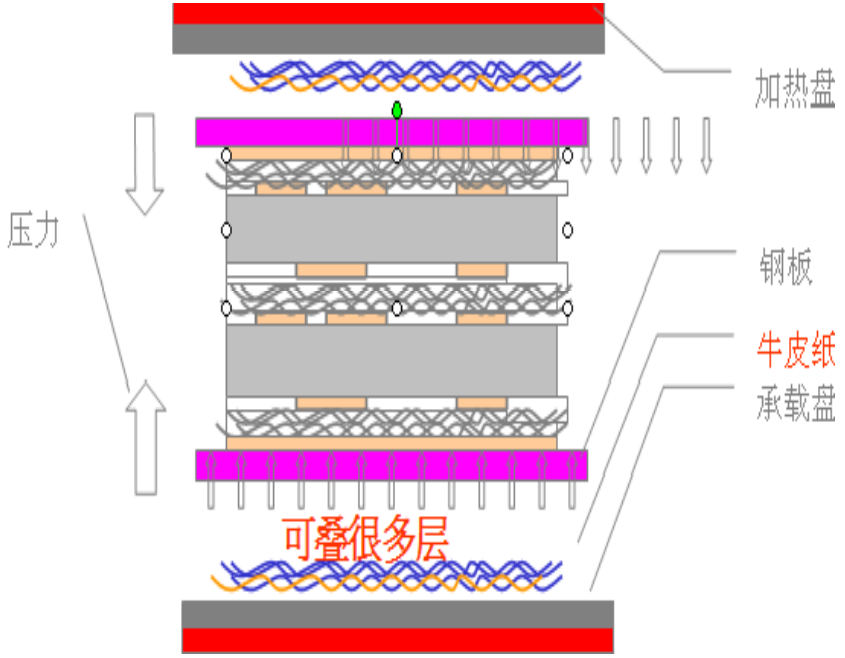
Riveting (for Lamination)

Lamination Process	Process Principle	Riveting Diagram
Riveting/Fusion	- Riveting: Use rivets to fasten multiple inner layers and PP together to prevent inter-layer slippage during subsequent processing. - Fusion: Heat the fusion window area on the board edge to bond with PP, further preventing inter-layer slippage.	

Stacking (for Lamination)

Lamination Process	Process Principle (Purpose)	Diagram (After Stacking)
Stacking (for Lamination)	Stack PP and inner substrates into the required multi-layer structure to be laminated.	

Lamination (Pressing)

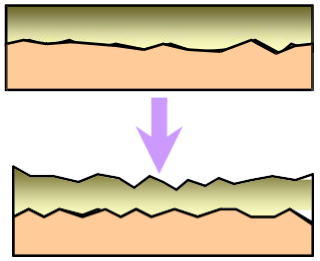
Lamination Process	Working Principle	Lamination Diagram
Pressing	Under high temperature and pressure, prepreg bonds copper foils together to form PCBs of different specified thicknesses.	

4、 Laser Drilling Process

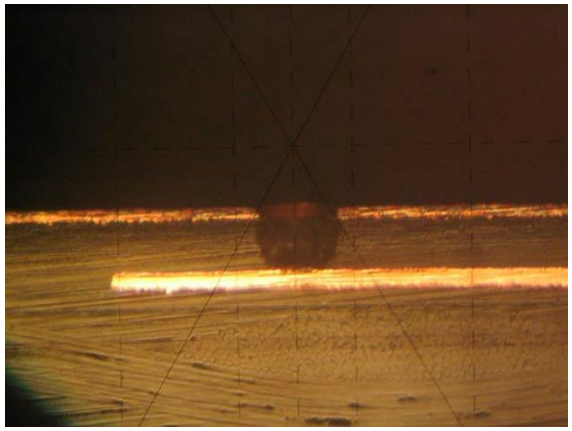
Flow: Brown Oxidation & Copper Reduction → Laser Drilling

Purpose:Reduce copper foil thickness to 7-8.5μm, perform brown oxidation, and drill blind vias on the copper surface using laser.

Brown Oxidation & Copper Reduction

Laser Process	Process Principle	Diagram (Before/After Brown Oxidation)
Brown Oxidation & Copper Reduction	Reduce copper thickness with copper reduction solution, then brown the copper surface to increase laser absorption, facilitating laser drilling.	 Before Brown Oxidation After Brown Oxidation

4、 4. Laser Drilling Process (Continued)

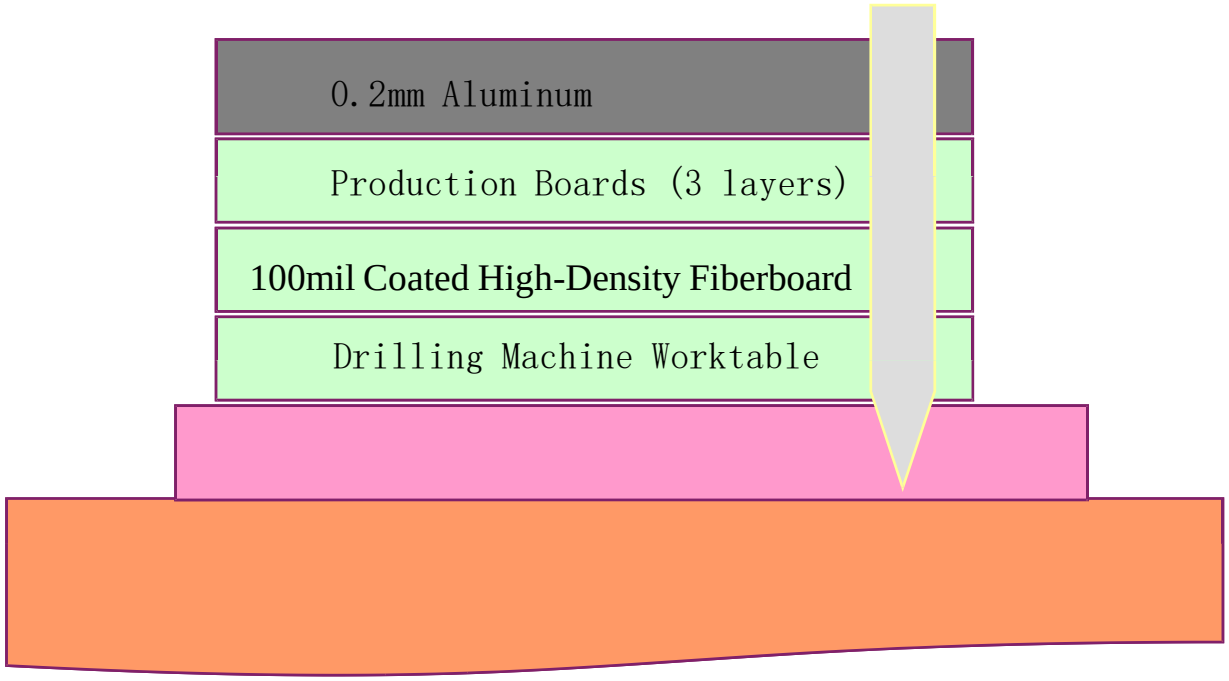
Laser Process	Process Principle	Diagram (After Laser Drilling)
Laser Process	Use laser to directly drill blind vias on the copper surface that has undergone copper reduction and brown oxidation.	

5. Drilling (Mechanical Drilling)

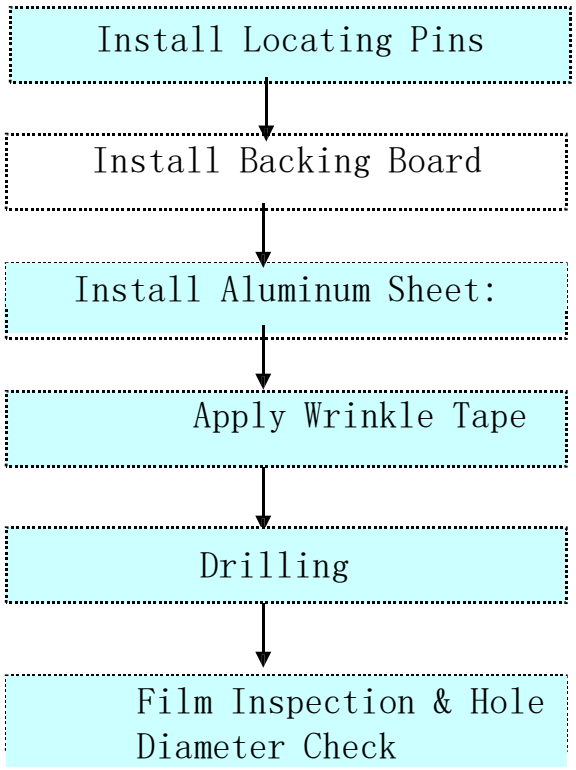
5.1 Purpose of Drilling

1.Drill holes as required by customers (position and size must meet specifications).
2.Realize inter-layer conduction and component insertion/soldering.
3.Drill positioning/alignment holes for subsequent processes.

5.2 Schematic Diagram of Mechanical Drilling Principle



5.3 Drilling Flow



Fix each stack of boards to the machine table for high drilling accuracy; pins must not be loose/bent and must match the diameter of positioning holes.

Prevent burrs during drilling, protect the machine table, and reduce drill bit wear; surface must be smooth/clean, debris must be small, and size must match the board to be drilled.

Prevent burrs on the top surface, protect the copper foil layer from pressure damage, improve hole position accuracy, and help cool the drill bit (reduce drilling temperature).

Fix the aluminum sheet and each stack of boards to the machine table for high drilling accuracy.

The CNC system controls the machine table to move along X/Y/Z axes according to the drilling program (drill tape) with given hole position coordinates.

Use film to check for missing holes and verify hole size.

5.4 Key Process Control Parameters for Mechanical Drilling

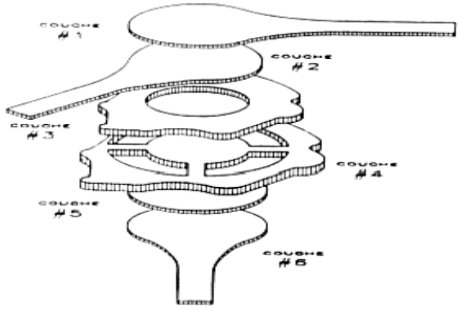
- Drill Rotational Speed (S): Affects cutting speed (V) (unit: Kr/min)
- Feed Rate/Retract Rate (F): (unit: mm/min)
- Maximum Hole Count (H): Max hits per drill bit
- Number of Boards per Stack (PL/STK): Panels per stack
- Drill Bit Re-grinding Times

6. PTH (Plated Through-Hole)

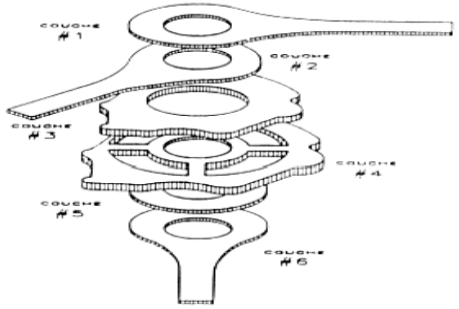
6.1 Purpose of PTH

Metallize non-conductive resin and glass fiber on hole walls to enable subsequent copper electroplating, forming conductive and solderable metal hole walls.

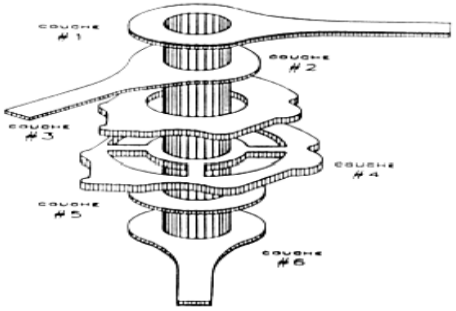
After Lamination



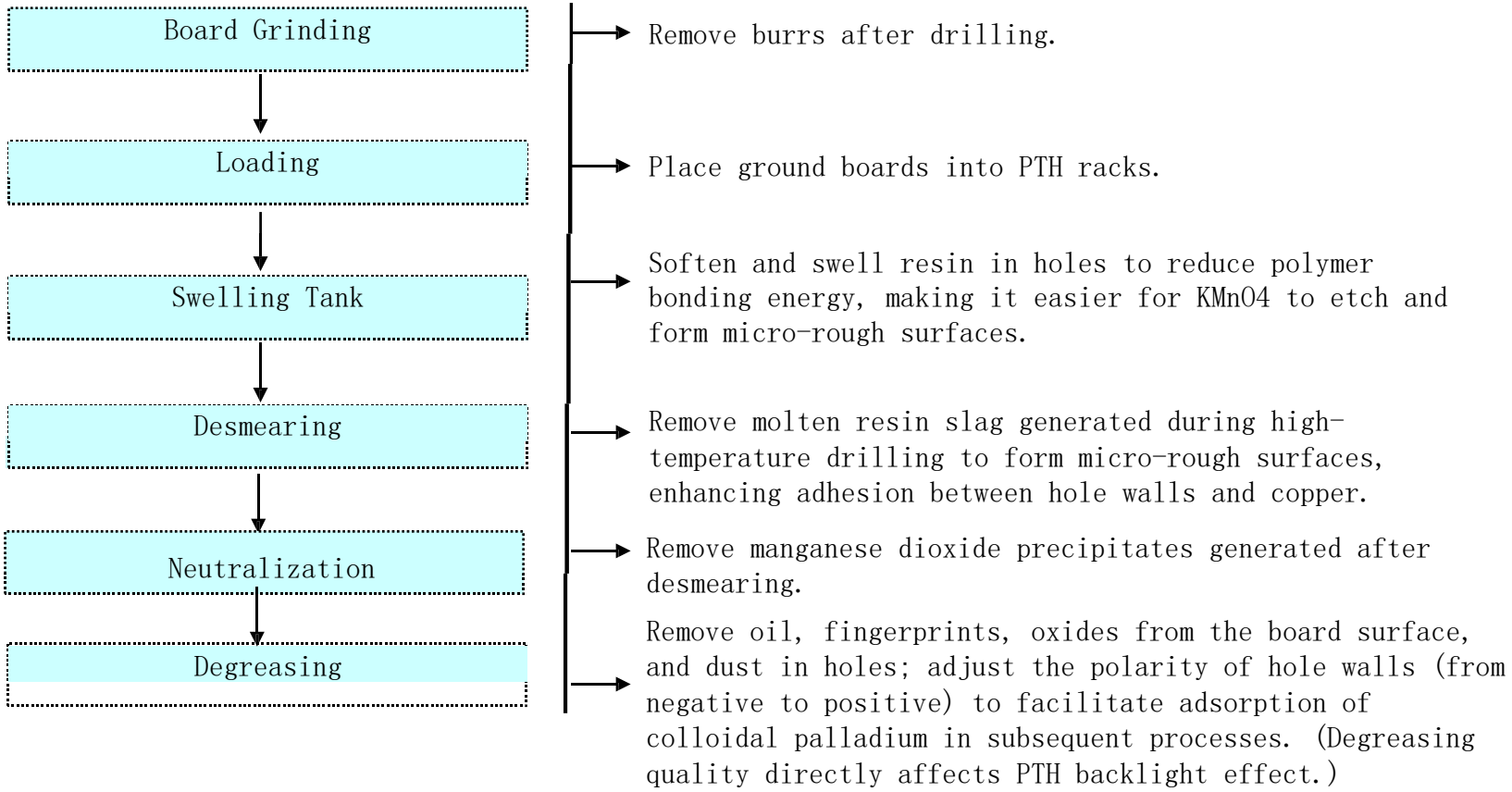
After Drilling



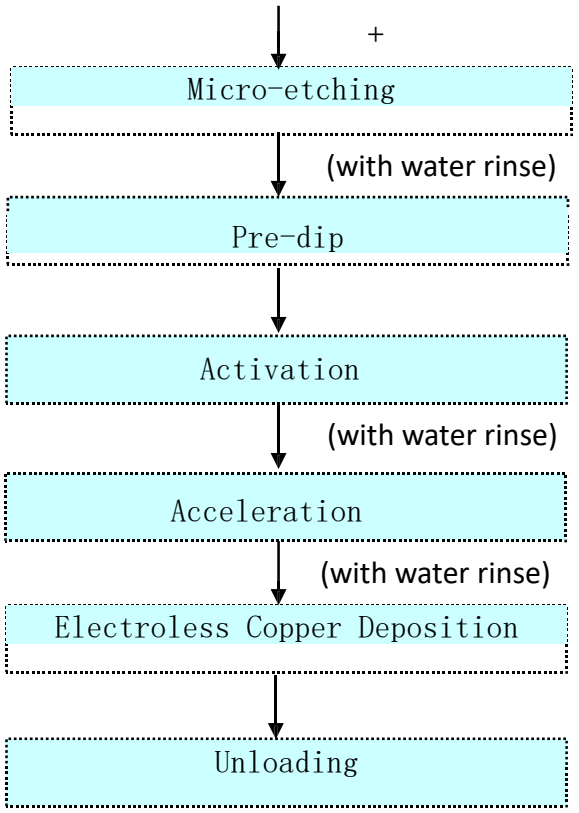
After PTH



6.2 PTH Flow


Board Grinding
Loading
Swelling Tank
Desmearing
Neutralization
Degreasing
Remove burrs after drilling.
Place ground boards into PTH racks.
Soften and swell resin in holes to reduce polymer bonding energy, making it easier for KMnO4 to etch and form micro-rough surfaces.
Remove molten resin slag generated during high-temperature drilling to form micro-rough surfaces, enhancing adhesion between hole walls and copper.
Remove manganese dioxide precipitates generated after desmearing.
Remove oil, fingerprints, oxides from the board surface, and dust in holes; adjust the polarity of hole walls (from negative to positive) to facilitate adsorption of colloidal palladium in subsequent processes. (Degreasing quality directly affects PTH backlight effect.)

PTH Flow:



Remove surface oxides, roughen the board surface to ensure good adhesion between the subsequent electroless copper layer and base copper; the newly formed copper surface has strong activity for effective colloidal palladium adsorption. (Also protects the palladium tank from contamination by pre-treatment solutions, extending its service life.)

Composition is similar to the palladium tank (except palladium chloride); effectively wets hole walls to ensure sufficient activation in the subsequent activation step.

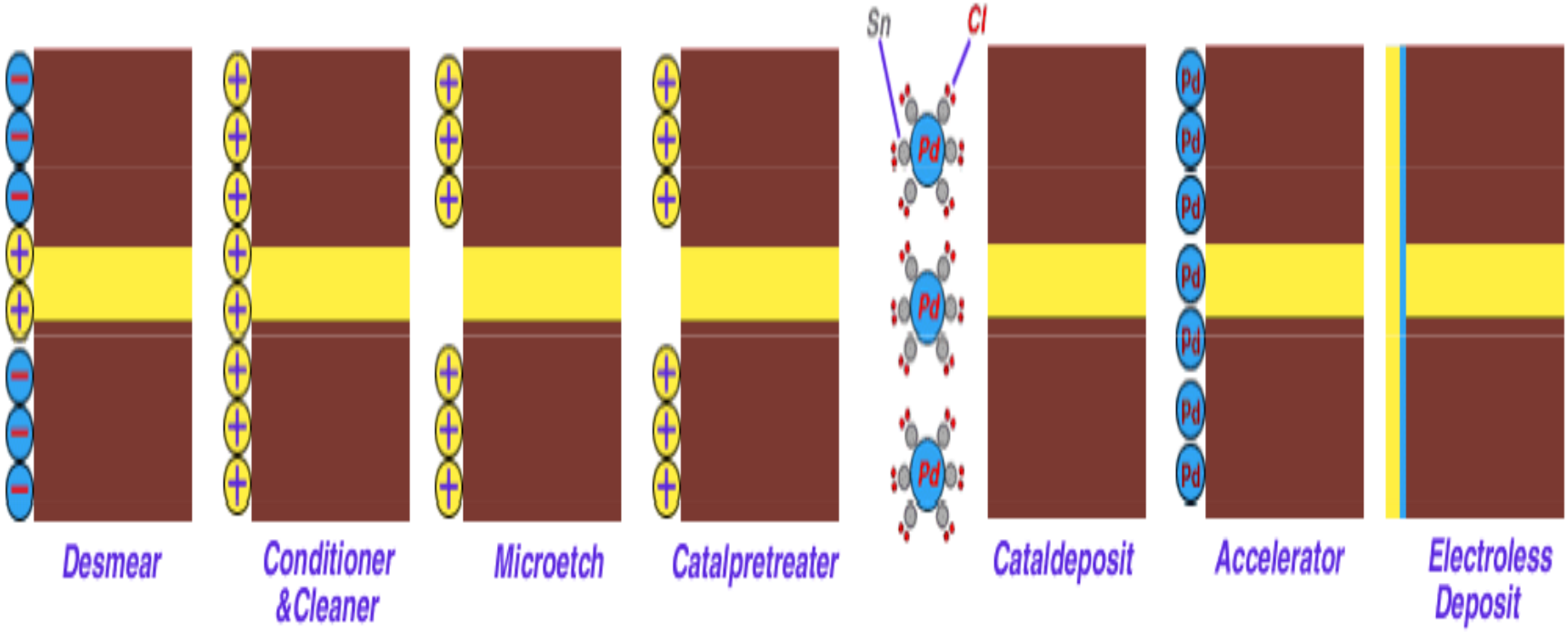
Positively charged hole walls (after alkaline degreasing) adsorb negatively charged colloidal palladium particles to ensure uniformity, continuity, and density of subsequent electroless copper.

Remove stannous ions surrounding colloidal palladium particles to expose palladium nuclei, which directly catalyze the electroless copper reaction.

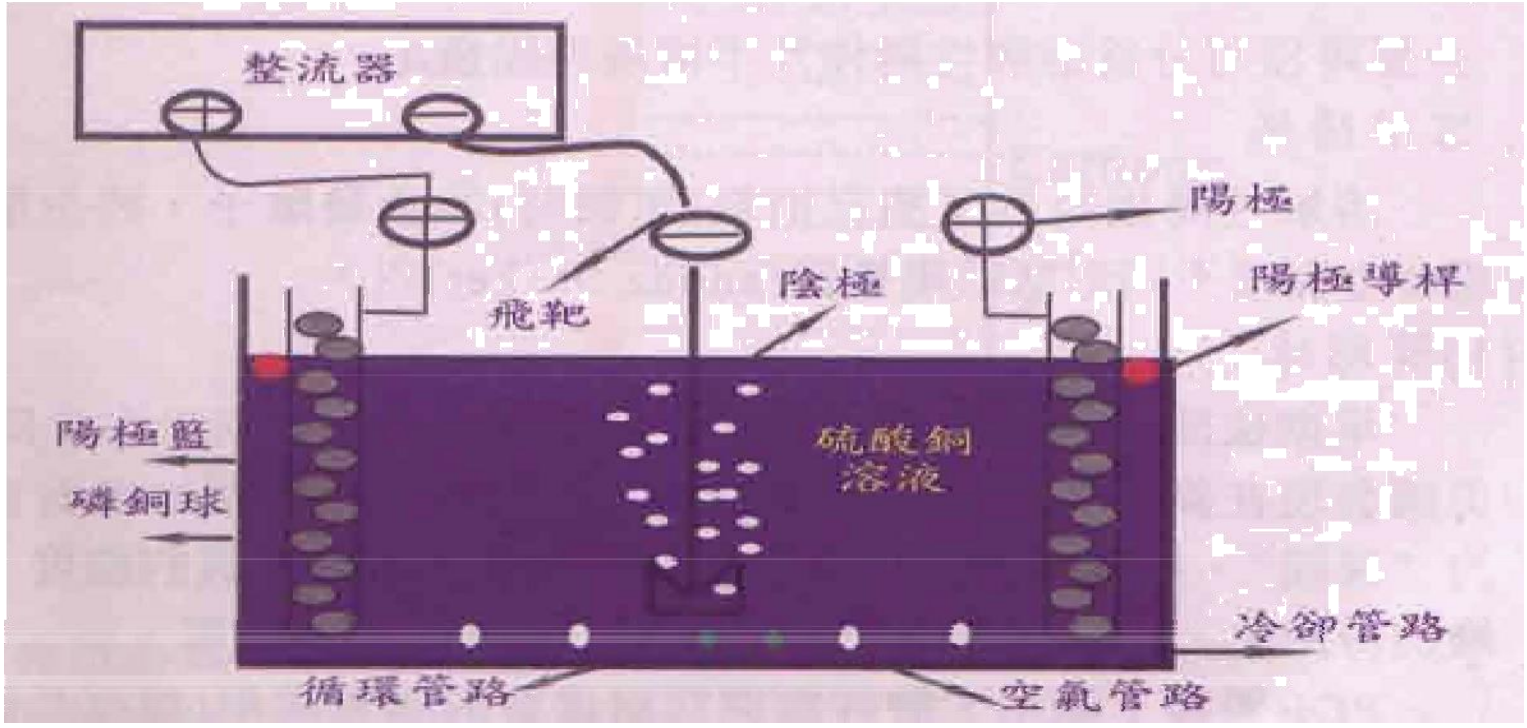
The palladium nuclei trigger the self-catalytic electroless copper reaction; newly formed copper and by-product hydrogen act as catalysts to sustain the reaction, depositing a layer of electroless copper on the board surface and hole walls.

Remove boards after PTH.

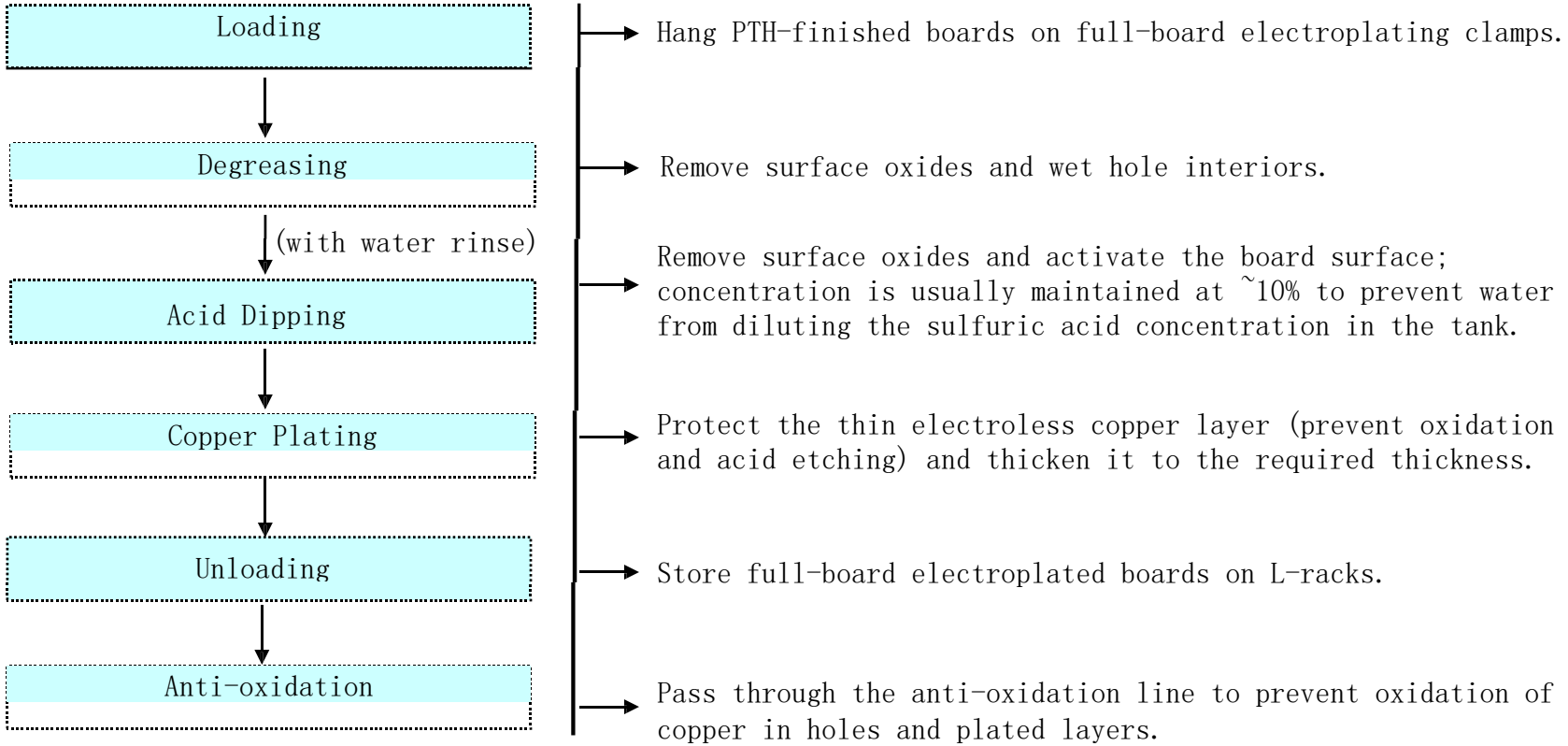
6.3 Principle of Electroless Copper (PTH)



Design Principle of Full-Board Copper Electroplating Tank



6.5 Full-Board Electroplating Flow

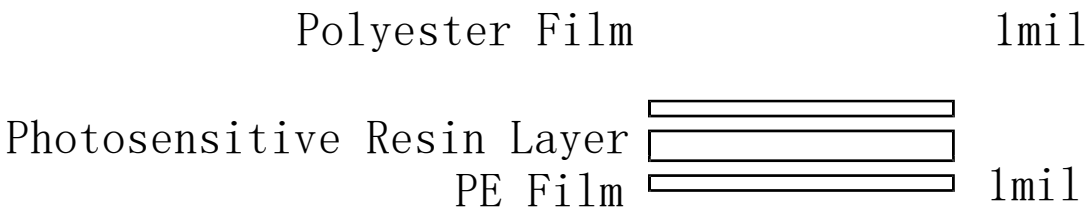


7. Outer Layer Fabrication Principle

7.1 Introduction to Dry Film

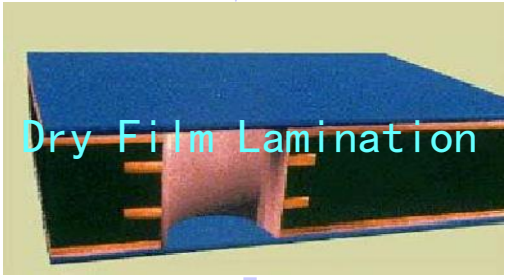
Dry Film (DRYFILM): A photosensitive material that undergoes polymerization after exposure, enhancing its resistance to weak alkalis (e.g., sodium carbonate). Unpolymerized dry film is easily dissolved by sodium carbonate solution.

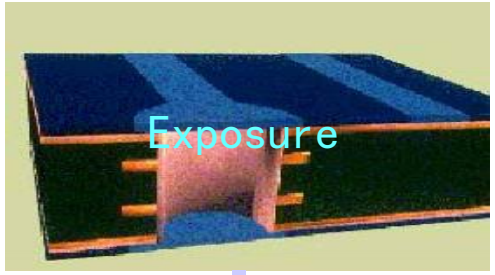
As the resist used in pattern transfer, it consists of three layers:

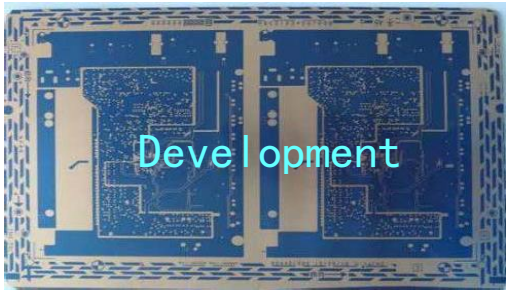


7.2 Pattern Transfer Principle

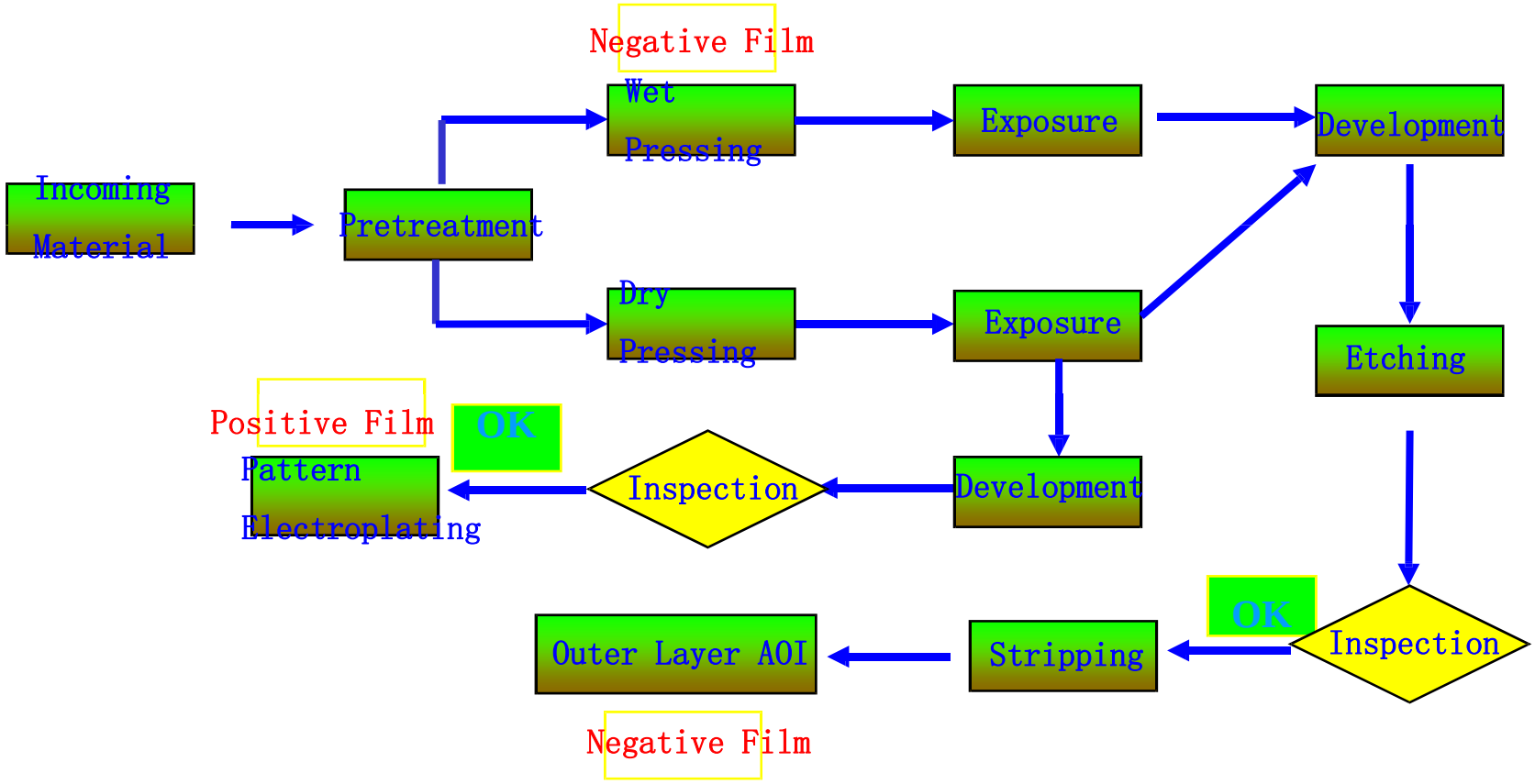
The process of transferring patterns from films to boards using photosensitive materials.



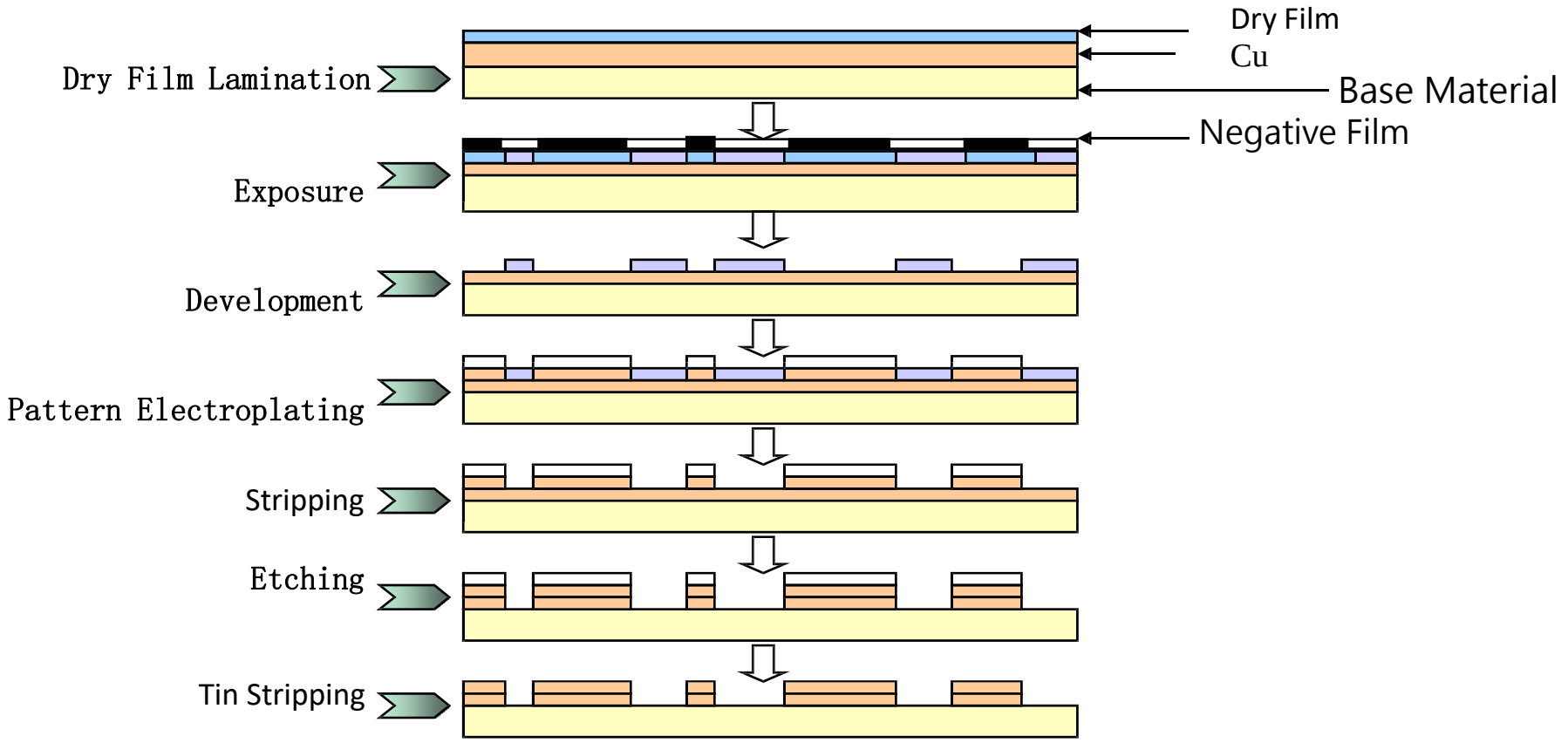




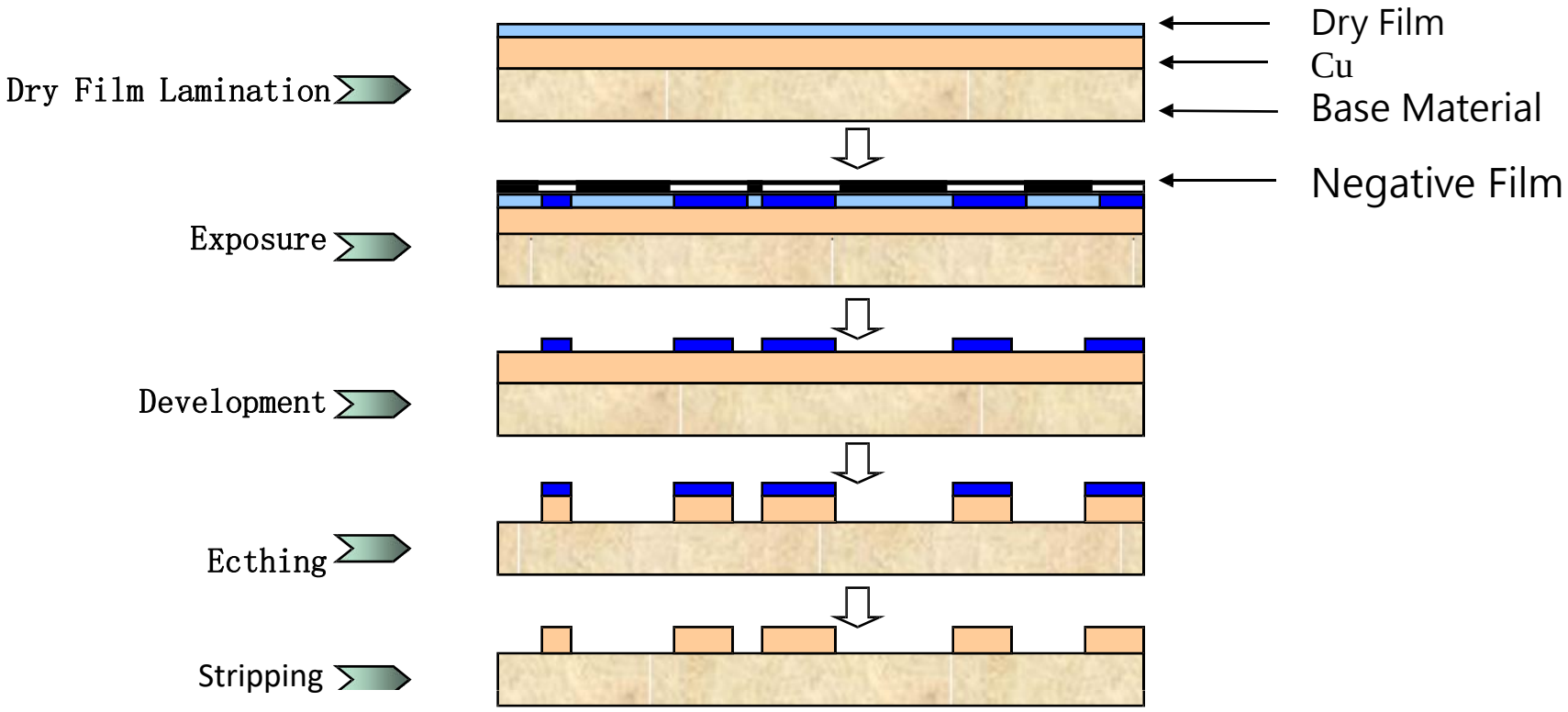
7.2 Pattern Transfer Flow



Pattern Transfer Principle (Positive Film + Alkaline Etching)



Pattern Transfer Principle (Negative Film + Acid Etching)

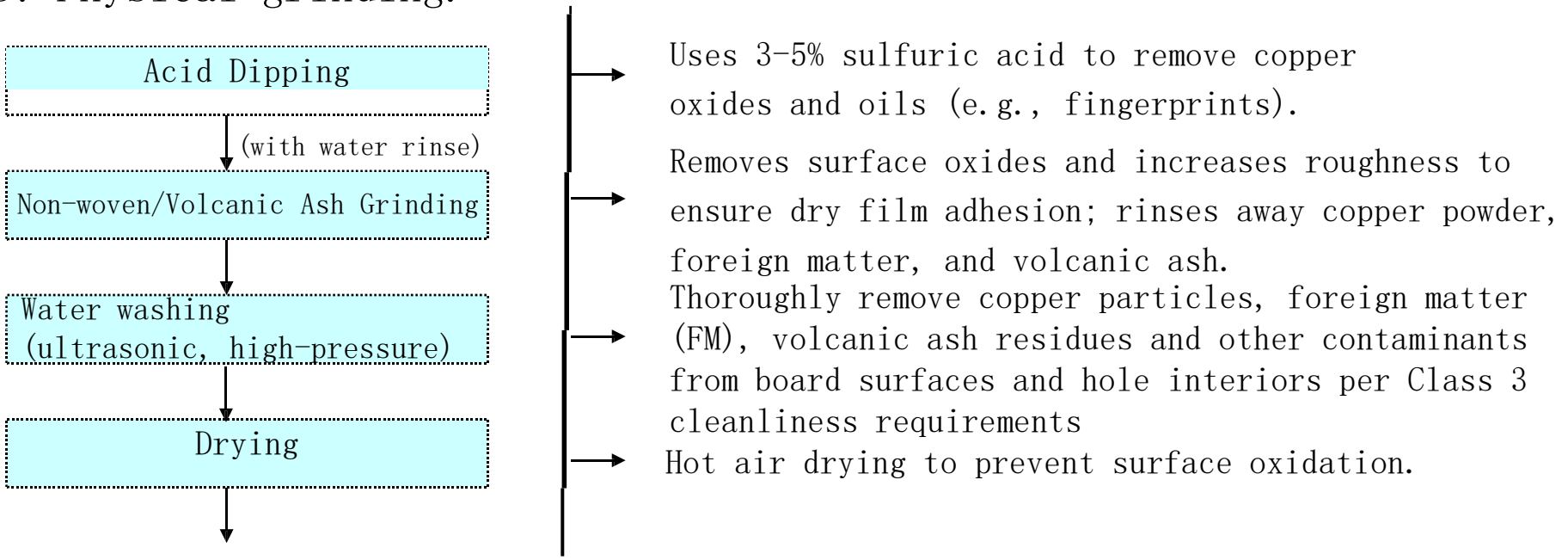


7.3 Outer Layer Circuit Flow (Positive Film)

Pretreatment

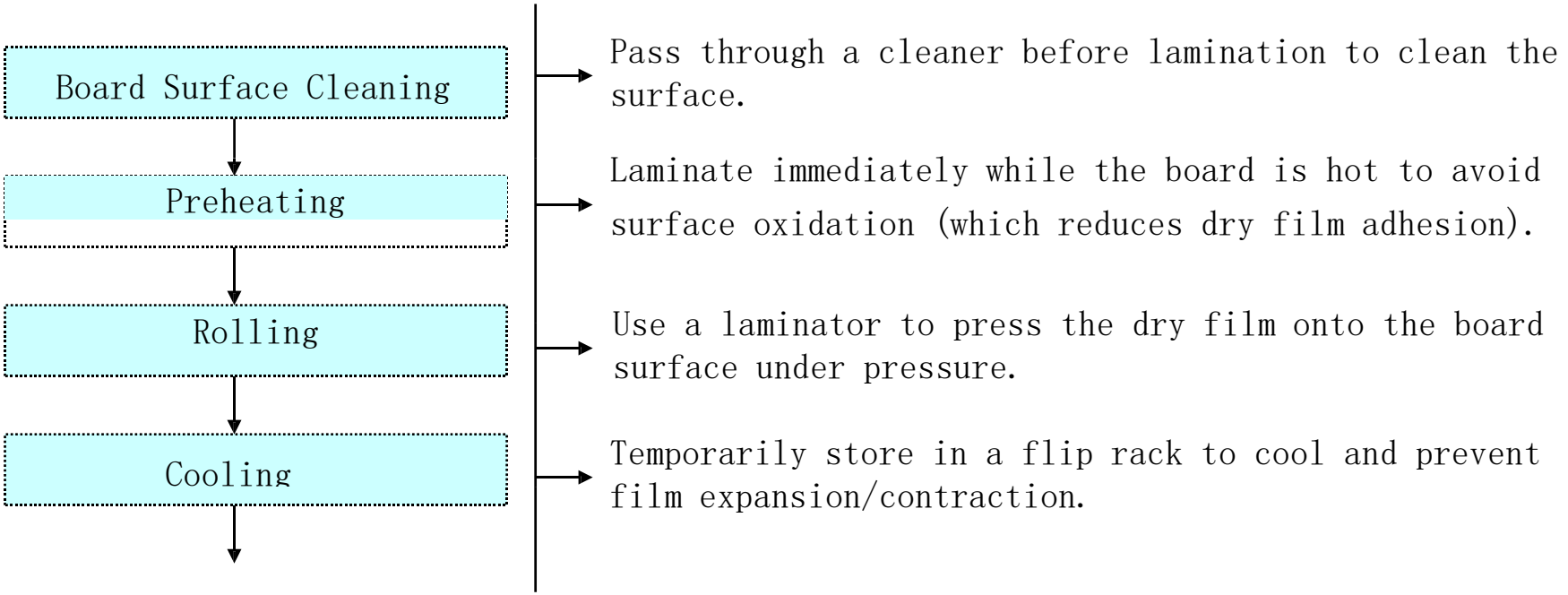
Definition: Board grinding cleans the surface, removes oxides, roughens the board, and enhances dry film adhesion.

Methods: Physical grinding.



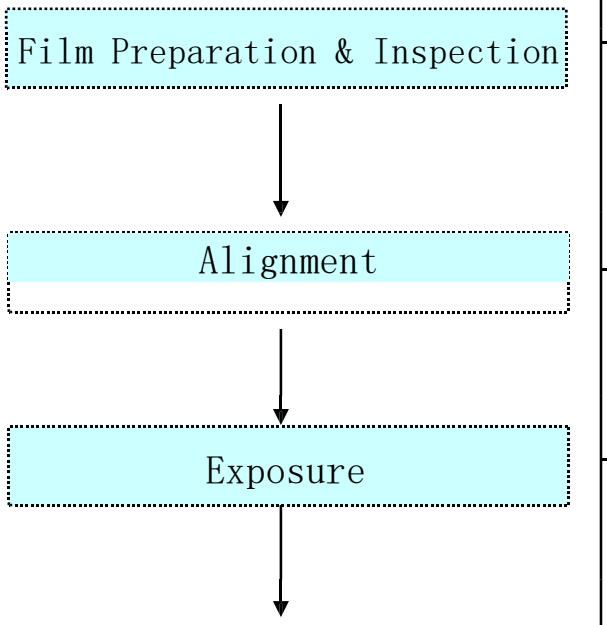
Dry Film Lamination

Principle: Use a laminator to adhere dry film to the roughened board surface via hot pressing.



(Image transter)

Exposure: By irradiating with ultraviolet light and using red film or black film, transfer the graphics required by the customer to the plate.

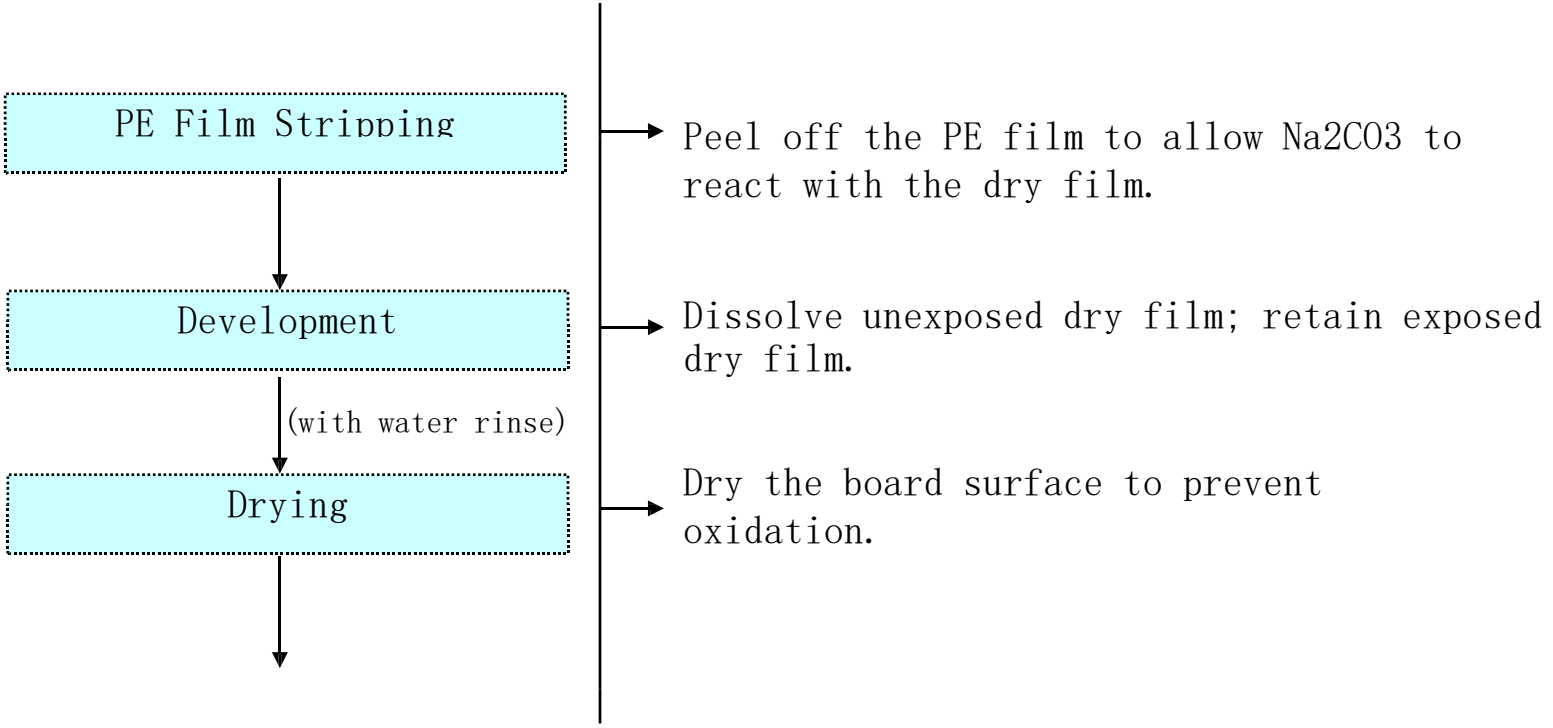


Red Film Production: Photosensitive film; exposed areas show no color change after ammonia treatment, while unexposed areas turn red (red areas block UV penetration).

Align the board with the film using positioning holes drilled earlier.

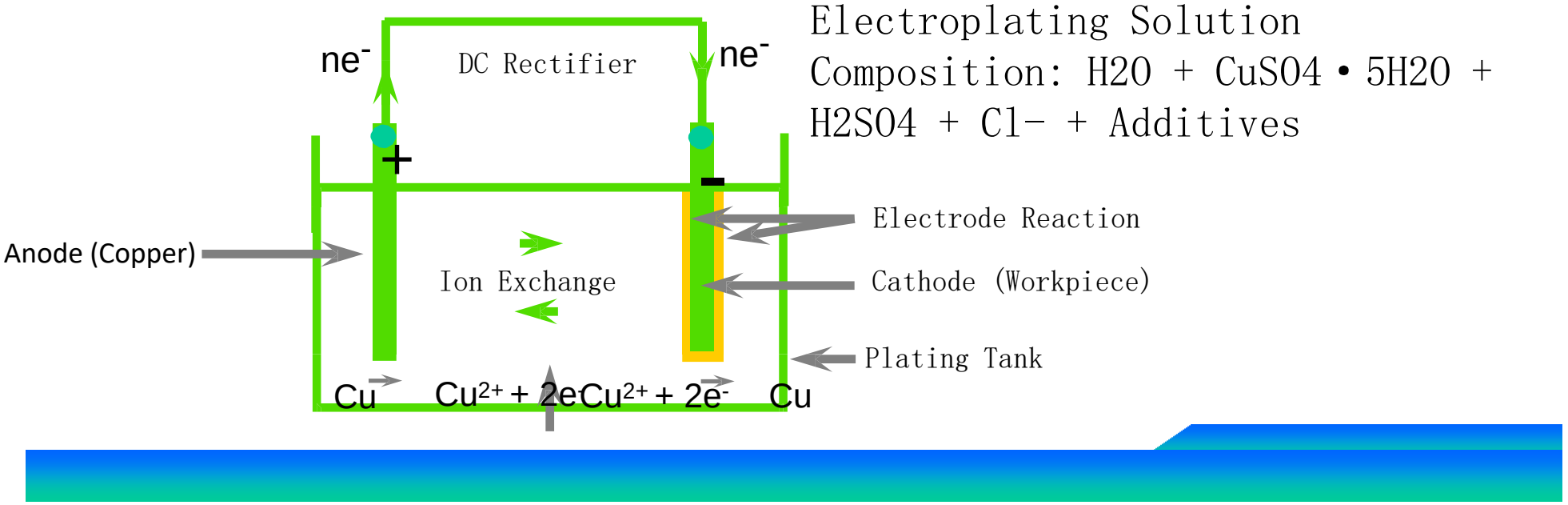
xposure Energy: 7-9 levels (excessive energy causes reflection and incomplete development; insufficient energy causes poor curing and over-development).
Vacuum Degree: Must reach ⩾600mmHg.

Development: Use Na2CO3 aqueous solution to dissolve unexposed dry film; exposed dry film remains—revealing the required pattern.



Pattern plating

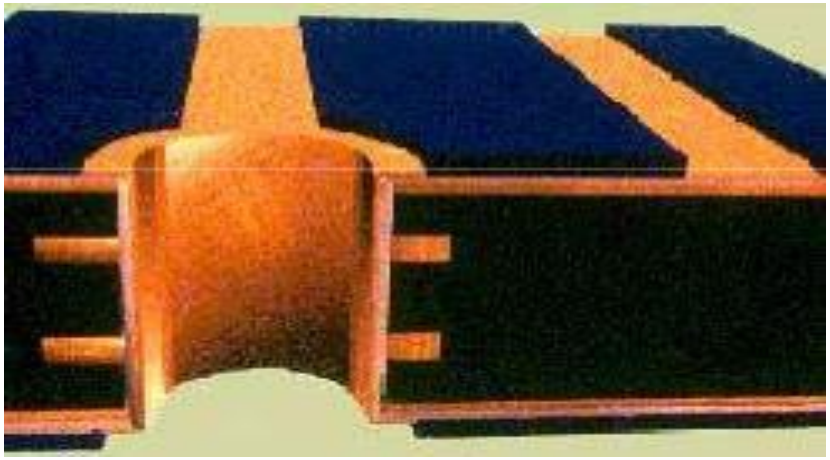
Purpose & Principle: Deposit copper on the electroless copper layer via electrolysis to provide sufficient conductivity/thickness, prevent thermal/mechanical defects in circuits, and serve as a base for pattern tin/nickel plating (thickness: 20-25μm, called "pattern copper plating").



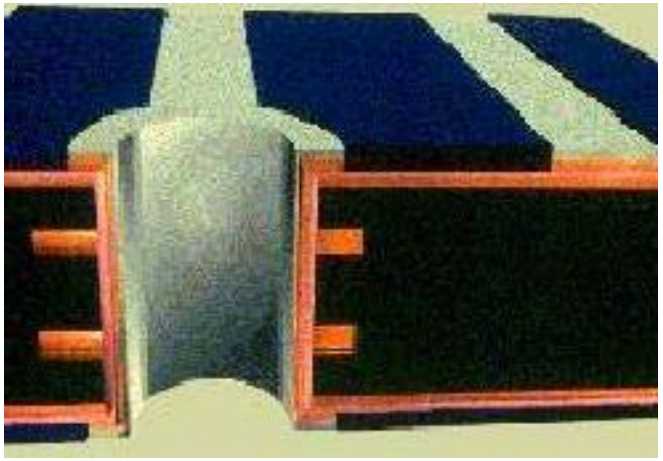
Electroplating Solution Composition: H2O + CuSO4·5H2O + H2SO4 + Cl- + Additives

Pattern Electroplating Diagram

The process of electroplating metallized holes and partial patterns to the required copper thickness and tin plating is called "pattern electroplating".



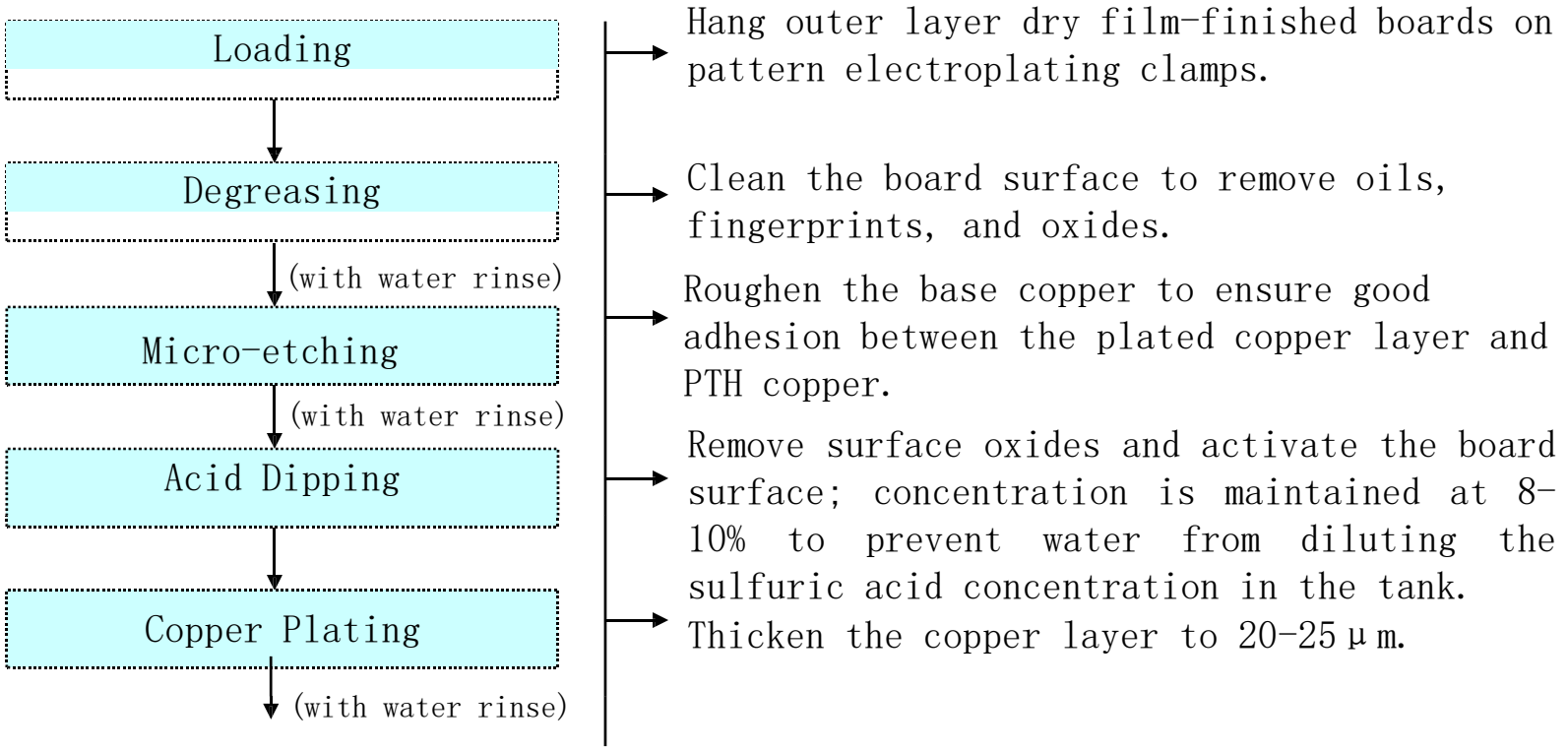
Pattern Copper Plating



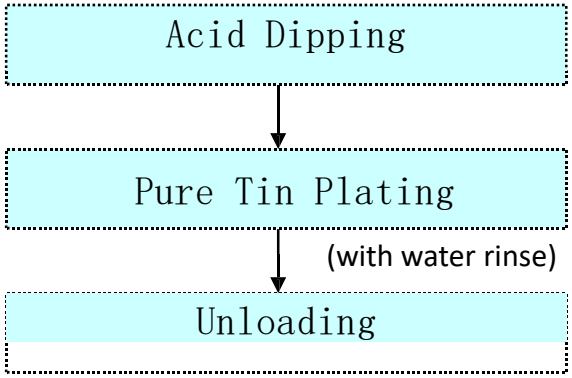
Pattern Tin Plating

Pattern plating

Pattern Electroplating Flow



Pattern Electroplating Flow



Remove surface oxides and activate the board surface; concentration is maintained at 8-10% to prevent water from diluting the sulfuric acid concentration in the tank.

Form an anti-etching layer for alkaline etching to create clear circuit patterns (thickness: 4-10μm).

Place pattern electroplated boards on L-racks.

Mechanism of Copper Electrodeposition in Acid Sulfate Baths

Electrode Reaction	Standard Electrode Potential
Cathode : Cu2+ +2e⌫Cu	φ。 Cu2+ / Cu = +0.34V
Side Reaction: Cu2+ + e⌫Cu ＋Cu+ + e⌫Cu	φ。 Cu2+ / Cu ＋ = +0.15V φ。 Cu+ / Cu = +0.51V
Anode : Cu -2e ⌫ Cu2+	

Cu - e ⌫ Cu+

2Cu+ + 1/2O2 + 2H+ ⌫2Cu2+ + H2O

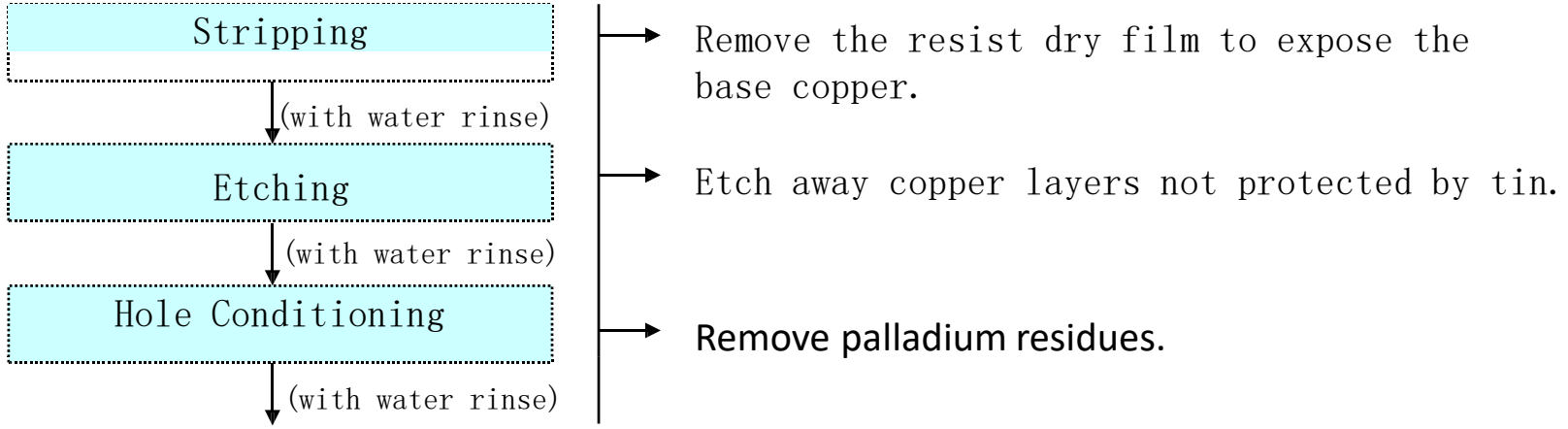
2Cu+ + 2 H2O ⌫2CuOH + 2H+

2Cu+ ⌫ Cu2+ + Cu

Circuitry etching

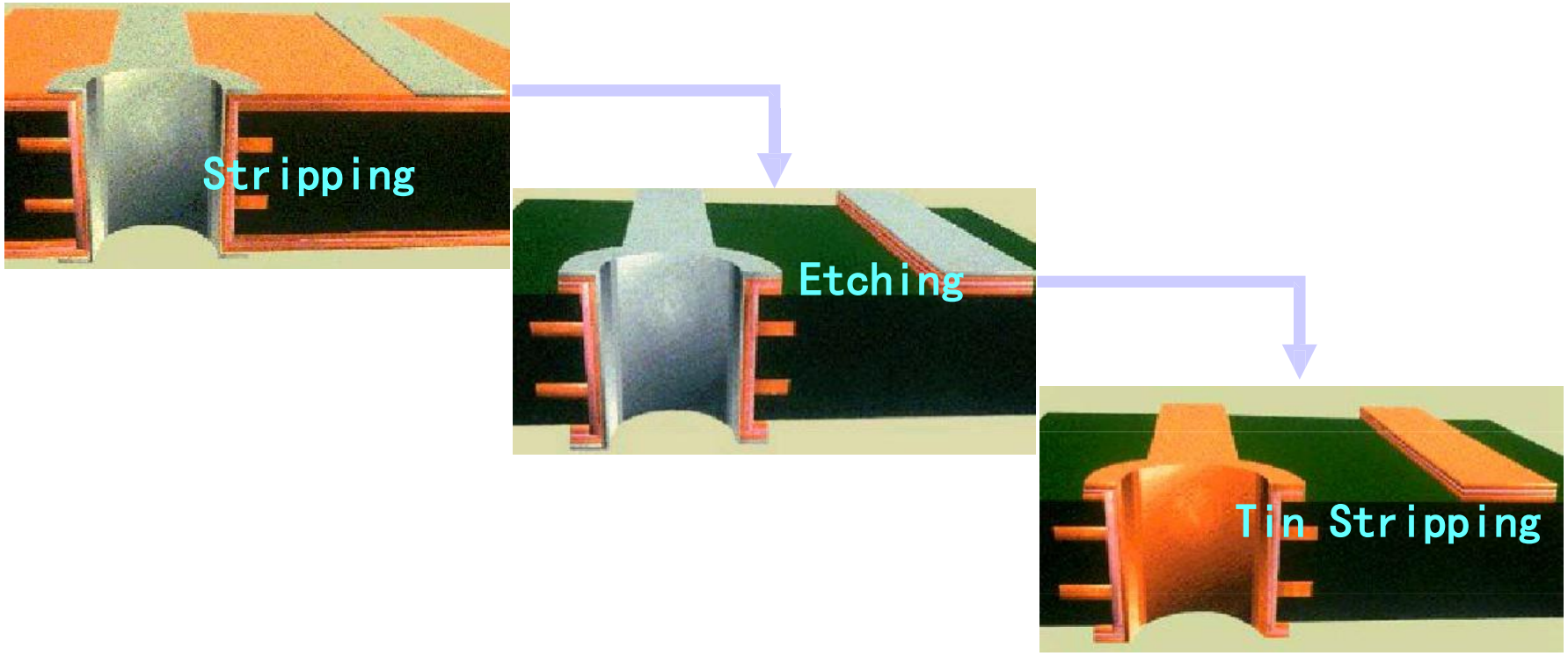
Purpose:Etch away non-circuit base copper to obtain the finished circuit pattern and achieve basic conductivity.

Flow:

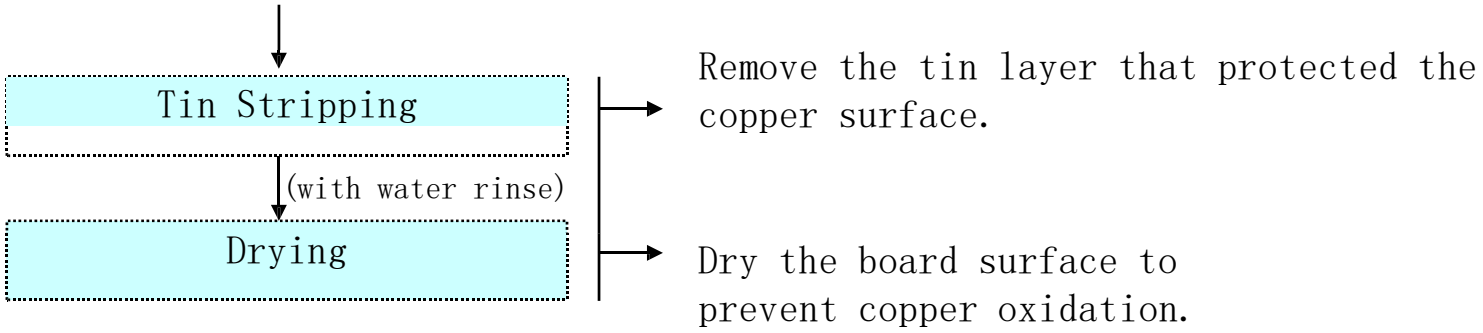


Etching Diagram

Etch away non-conductive copper areas.



Circuitry etching



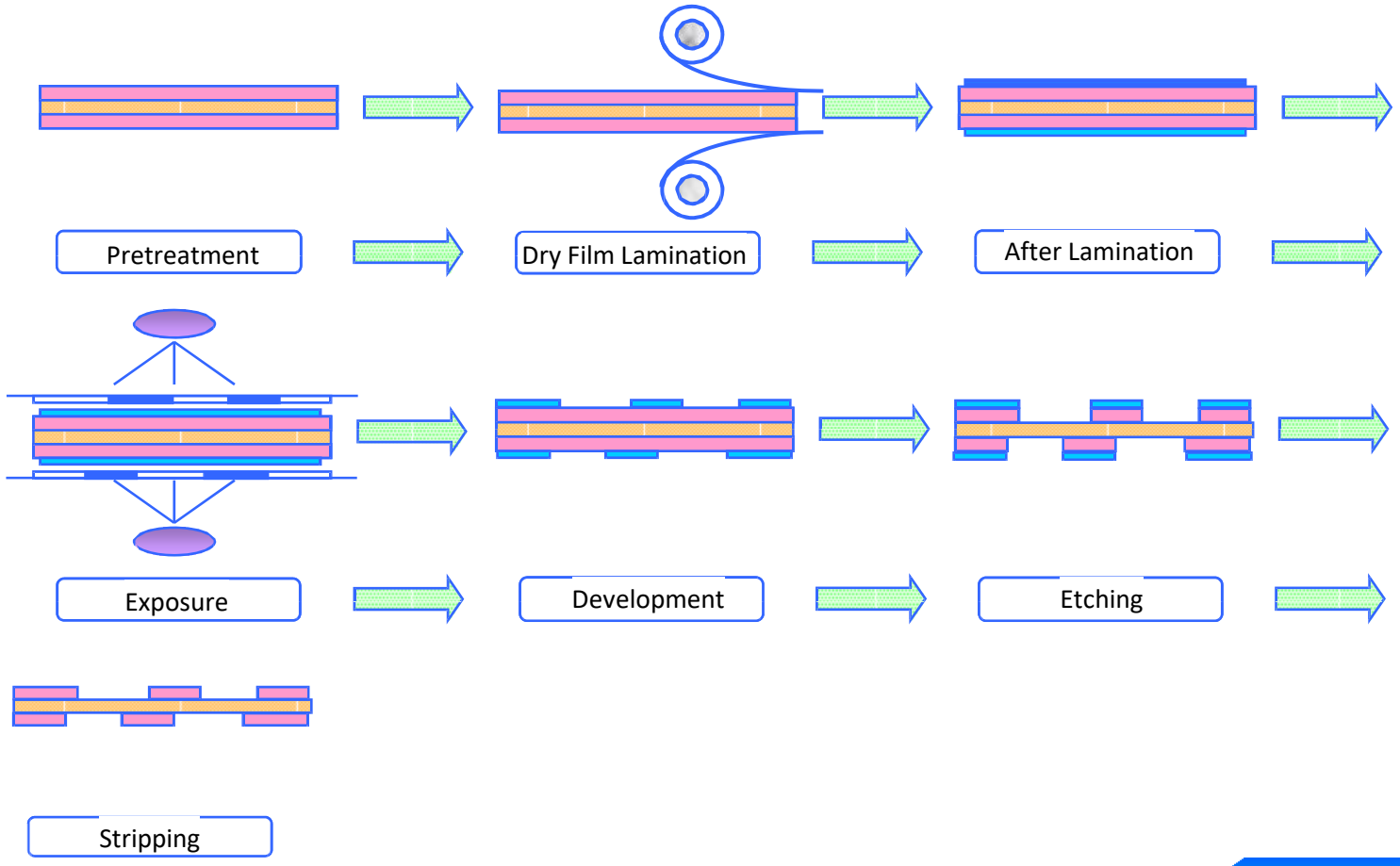
Basic Principle of Stripping:

1. Exposed dry film is a polyester polymer with a cross-linked three-dimensional network structure containing carboxyl groups (-COOH).

2. It undergoes saponification with special stripping solution, breaking the long-chain network structure.

3. Broken fragments are stripped from the copper surface under high pressure.

7.4 Outer Layer Circuit Flow (Negative Film)

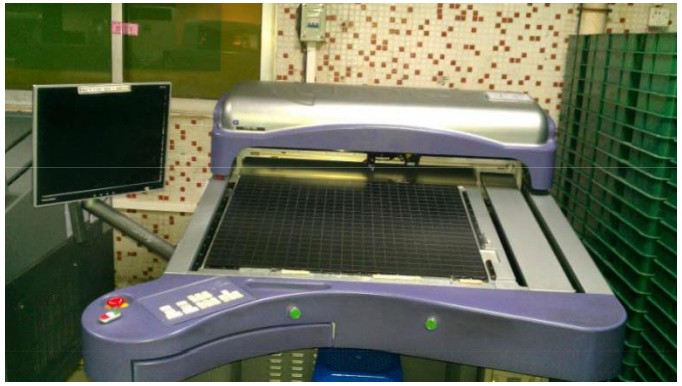


8. Outer Layer AOI Inspection

AOI (Automatic Optical Inspection): Uses optical reflection to feed board images to the device, comparing them with preset logical judgment rules or data patterns to identify defect locations.

VRS (Verify & Repair Station): Confirms and repairs defects detected by AOI through AOI-connected test data.

AOI



VRS

In simple terms: AOI identifies board defects; VRS assists in repairing defects.

Inspection Method	Purpose	Notes
AOI: Automatic Optical Inspection	Transfer board images to the device via optical principles, compare with preset logical rules or data patterns to locate defects.	Uses logical comparison, so false positives may occur; manual confirmation is required.
V.R.S: Verify Repair Station	Receive test data of each board from AOI (via connection), confirm and repair AOI-detected defects manually.	VRS operators not only confirm defects but also repair repairable defects directly.

9. Solder mask

Process Principle:

Solder mask (resist) layers are formed by overall printing with photosensitive ink. Precision solder mask patterns (made from photographic films) are exposed to UV light, then developed with weak alkaline solutions (sodium/potassium ions) to expose solder pads requiring soldering.

Functions of Solder Mask Ink:

1. Insulation 2. Prevention of copper oxidation 3. Aesthetics

Composition of Liquid Photosensitive Solder Mask Ink:

Base Agent: Epoxy acrylic resin, diethylene glycol ethyl ether acetate, high-boiling aromatic hydrocarbons, photosensitizers, additives, pigments, fillers.

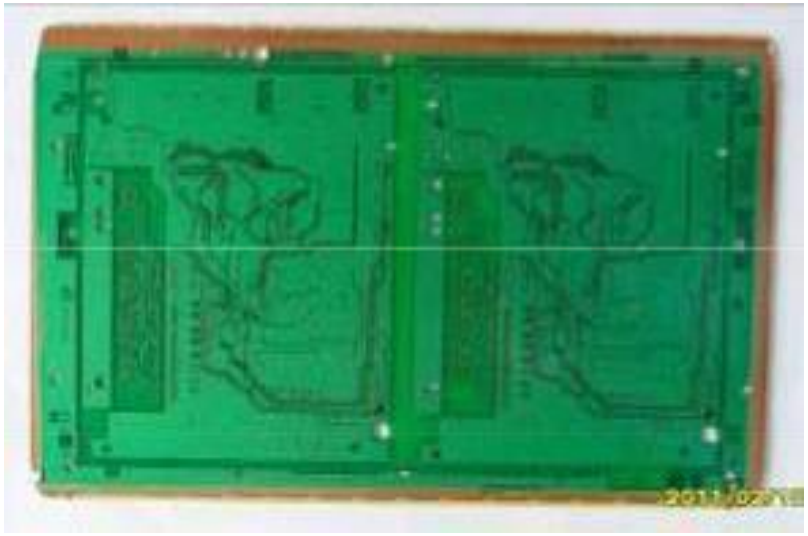
Hardener (Curing Agent): Epoxy resin, acrylic monomers, diethylene glycol ethyl ether acetate, high-boiling aromatic hydrocarbons.

Color Options:A. Green (dark, medium, light) | B. Blue | C. Black | D. Red | E. Yellow | F. White

Solder Mask Diagram

Solder mask involves coating the board surface with a layer of ink to achieve three functions: solder resistance, protection, and insulation.

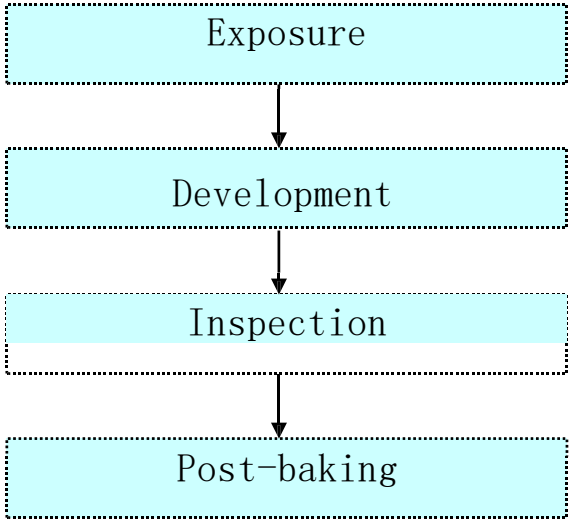
Before Solder Mask



After Solder Mask

9.1 Solder Mask Process Flow & Description

Process	Purpose	Materials & Equipment	Notes
Pretreatment	Remove surface oxides, increase surface roughness, and enhance adhesion between ink and copper.	Nylon brush, sandblasting /volcanic ash	The thermosetting solder mask ink used is two-component (base agent + hardener). After opening, mix the two components uniformly, let stand, then use. Initial viscosity after opening: ~200dps; viscosity increases after standing.
Printing	Coat the board with solder mask; expose solder pads/holes (for soldering) via exposure/development; cover other areas with solder mask to prevent soldering shorts.	Solder mask ink	
Pre-baking	Evaporate solvents in the ink, partially cure the ink, and prevent film sticking during exposure.	Pre-baking oven	



Use the UV-blocking property of film emulsion to cure the solder mask area via high-energy light sources; unexposed ink (in opening areas for soldering) is developed away with dilute sodium carbonate solution.

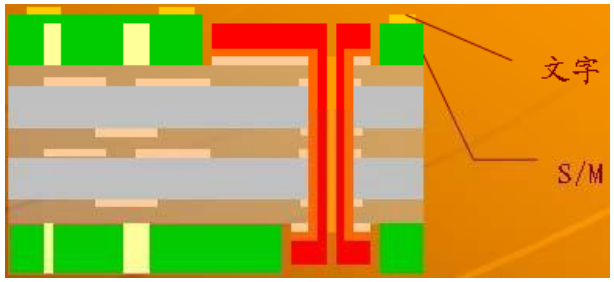
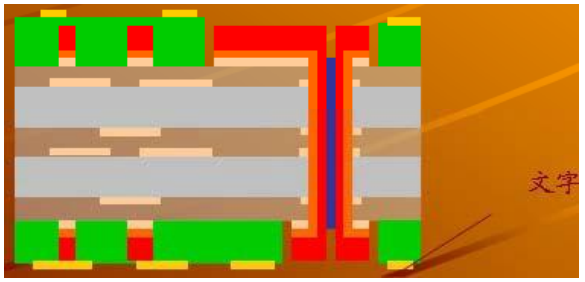
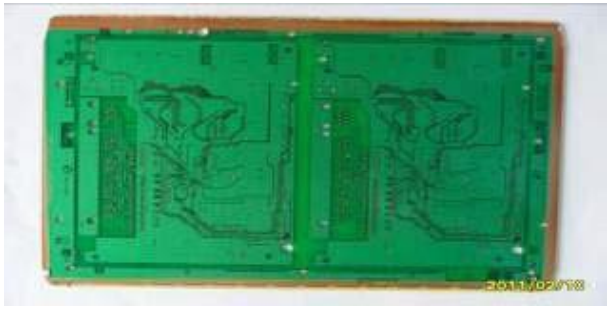
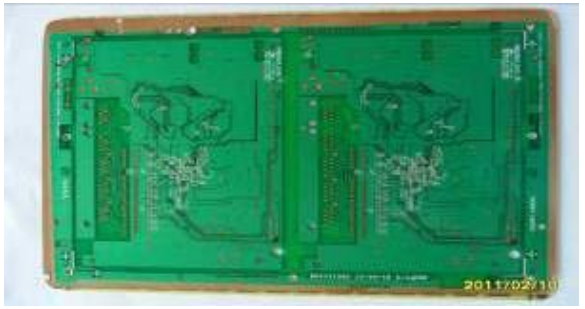
Use sodium/potassium ions to break down unexposed ink molecules (not cross-linked) into hydrophilic substances, which are dissolved and removed; exposed ink remains.

Check for solder mask defects (incomplete development, over-development, ink color issues, foreign matter on ink surface).

Achieve full curing via thermal curing, converting cross-linked medium molecules into a three-dimensional network structure.

Note: Most inks cure at 150° C for 60 minutes. However, due to ink properties (e.g., thickness), immediate high-temperature curing may cause wrinkling (upper ink cures while lower ink does not). For via-plugged ink, direct high-temperature baking causes rapid bubble expansion and solvent evaporation (before full curing), leading to ink overflow from vias.

10. Legend Printing

Flow	Purpose	Diagram
Print 1st→Baking→Print 2nd Side →Baking→Process Next Side	Facilitate component insertion identification and maintenance	    Before Legend After Legend

11. surface treatment

Process Principle:

According to customer requirements, treat the exposed copper pads (after solder mask) to form a protective layer on the copper surface—preventing oxidation/sulfidation, and enhancing bonding and conductivity between components and solder joints during electronic assembly.

Types of Surface Treatment Processes:

Surface Treatment	Thickness Range
Enig	Au: 0.025-- 0.1um, Ni(Min):2.54um
OSP	0.15--0.5um
Immersion Silver	≥0.15um
Hot Air Solder Leveling (HASL)	≥1um
Immersion Tin	≥0.8um
Hybrid Surface Processes	**ENIG+OSP，Gold Finger， Carbon+OSP， Gold Finger+OSP**

UGPCB ELECTRONICS CO., LIMITED

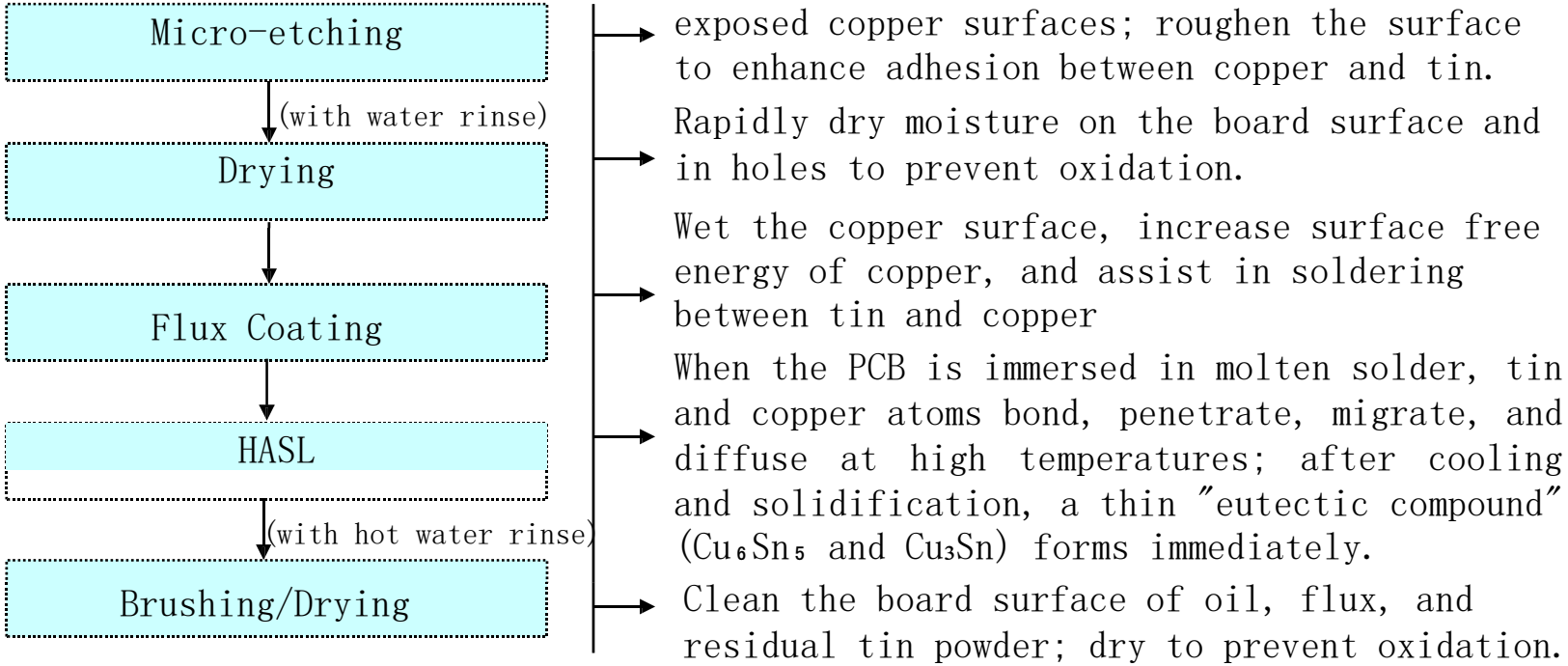
Comprehensive Comparison of Surface Treatment Processes

Item	HASL	OSP	Electroplated Ni/Au	ENIG	Immersion Silver
Flatness & Common Defects	Uneven thickness, "turtle back" phenomenon	**Flat surface, prone to scratches**	Poor thickness uniformity	Flatsurface, "black pad" phenomenon	Flat surface, "tin whisker" phenomenon
Soldering Strength	Excellent	Excellent	General	General	Good
Solder Joint IMC	Sn/Pb (Cu_6Sn_5)	Cu(Cu_6Sn_5)	Ni (Ni_3Sn_4)	Ni (Ni_3Sn_4)	Sn (Cu_6Sn_5)
Multiple Soldering Cycles	Multiple	≤3 cycles	Multiple	Multiple	Multiple
Shelf Life	6 months	3 months	12 months	6 months	3 months
Board Dimensional Stability	High-temperature impact, dimensional change	Stable	Stable	Stable	Stable
Process Stability	Unstable (affected by board structure)	Stable	Relatively stable	Relatively stable	Stable
Environmental Impact	**Lead-containing, harmful to the environment**	No environmental impact	No environmental impact	No environmental impact	No environmental impact
Cost-Efficiency	Low	Lowest	Highest	Highest	5-8× HASL
Waste Disposal	Environmental pollution, difficult to handle	Simple	Cyanide-containing, large waste volume, high disposal cost	Cyanide-containing large waste volume, high disposal cost	Simpler than ENIG
Thickness Range	3～7μm	0.3～0.5μm	Ni≥2.5μm Au: 0.05～0.15μm	Ni≥2.5μm Au: 0.03～0.076μm	0.8～1.2μm

11.1 Surface Treatment - Lead-Free HASL

Lead-Free HASL Flow:

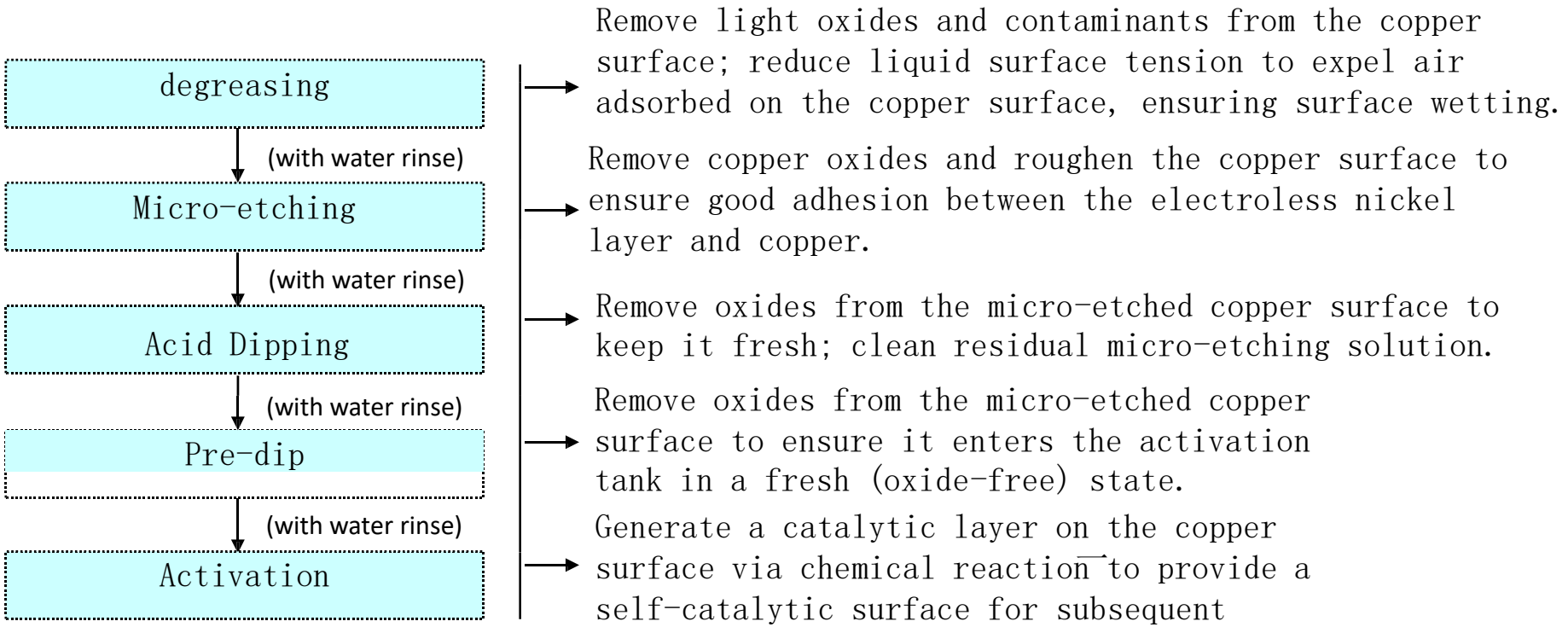
Also known as "solder leveling", it involves immersing the PCB in molten solder, then blowing off excess solder on the board surface and metallized holes with hot air to form a smooth, uniform, and bright solder coating (lead content < 0.1%).



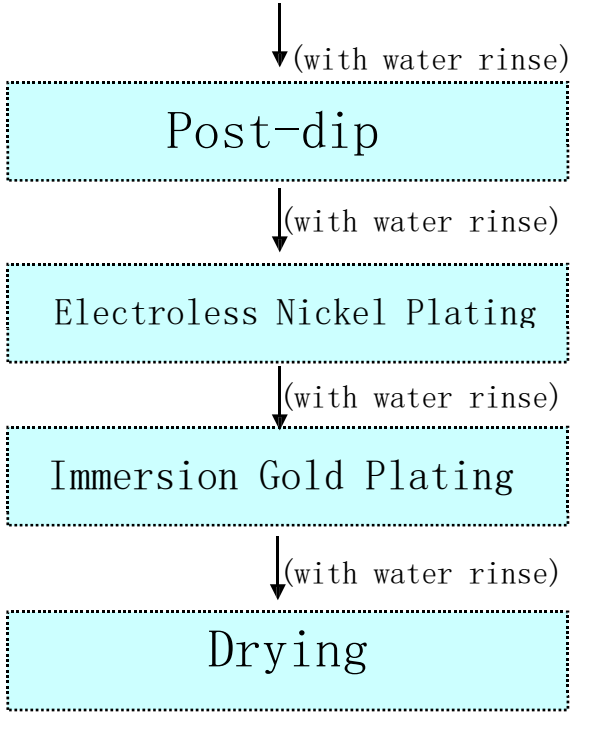
11.2 Surface Treatment – ENIG

ENIG Flow:

Chemically treat exposed copper pads (after solder mask) to deposit a thin gold layer (purity: 99.99%, hardness < 80 Knoop, density: 19.3g/cm³) on the copper surface.



ENIG Flow



Provide a metal diffusion barrier between copper and gold; act as a corrosion-resistant layer, solderable surface, and stable bonding layer for wire bonding.

Provide a metal diffusion barrier between copper and gold; act as a corrosion-resistant layer, solderable surface, and stable bonding layer for wire bonding.

Deposit a thin, uniform gold layer on the newly plated nickel layer via displacement reaction. The reaction stops when the nickel surface is fully covered by gold, so the gold layer has a thickness limit.

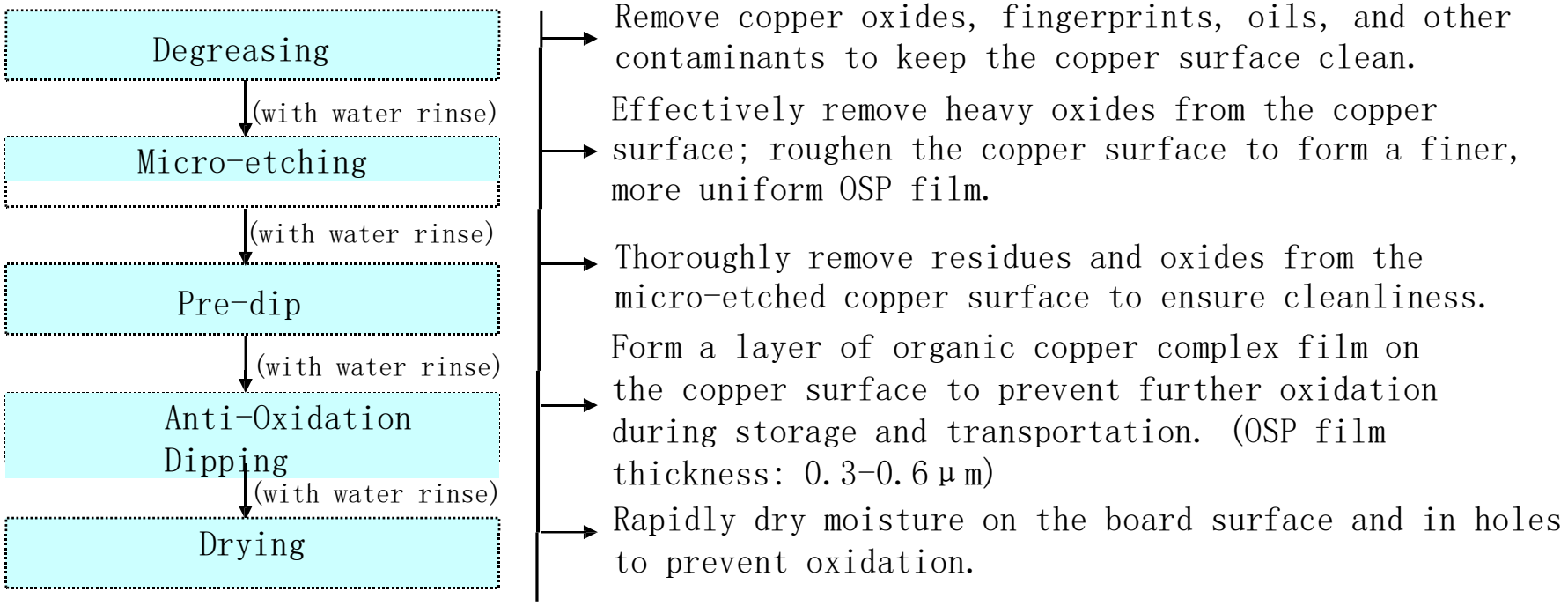
Function of Immersion Gold Layer: Protect the underlying nickel from oxidation and maintain solderability.

Dry moisture on the board surface and in holes to prevent oxidation.

11.3 Surface Treatment - OSP

OSP Flow:

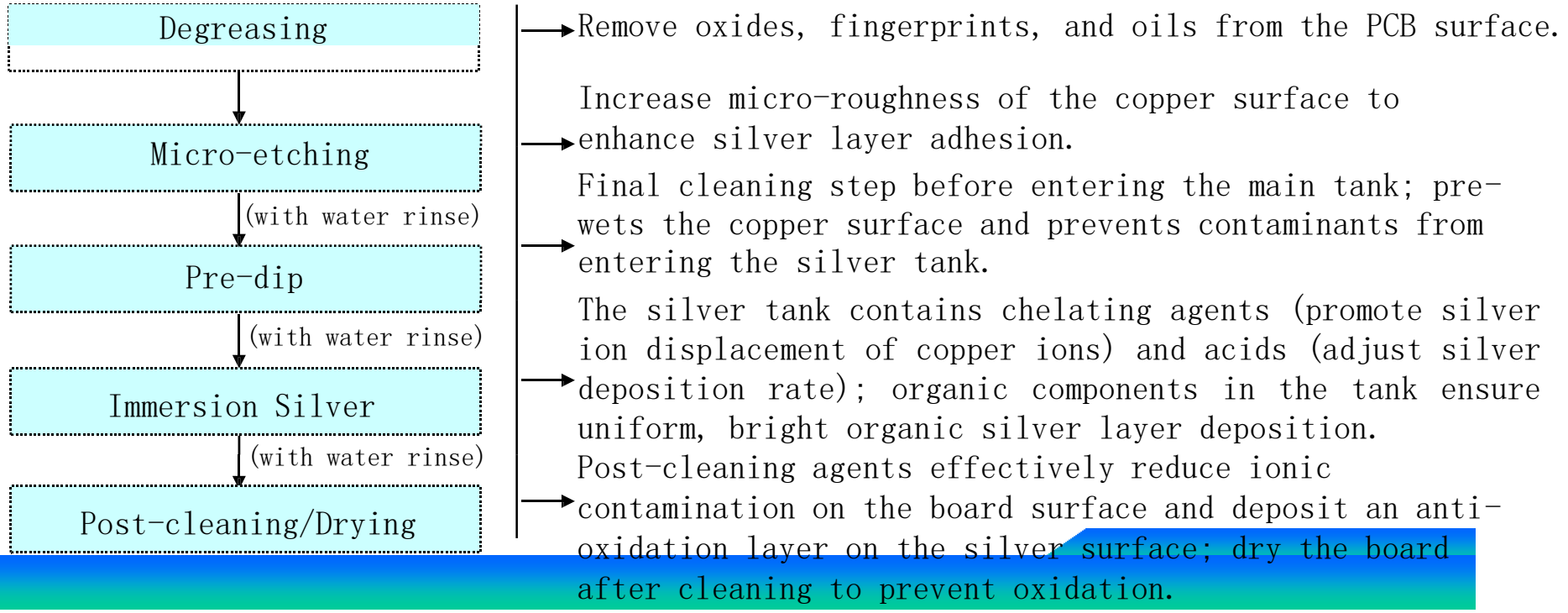
Coats exposed copper pads (after solder mask) with an organic solderability preservative to form a layer of organic copper complex film on the copper surface.



Surface Treatment - Immersion Silver

Immersion Silver Flow:

Silver is a white, soft, malleable, and ductile metal with the best thermal and electrical conductivity. It can be easily dissolved into ionic solutions for plating on surfaces requiring silver coating. Immersion silver is the process used to deposit silver on PCBs (silver thickness: ~0.1-0.5μm).



12. profiling

Purpose & Types of Profiling

Process semi-finished PCBs into the required outer dimensions specified by customers.

Types:

Routing: Use high-speed rotating routing bits to cut PCBs to the required shape.

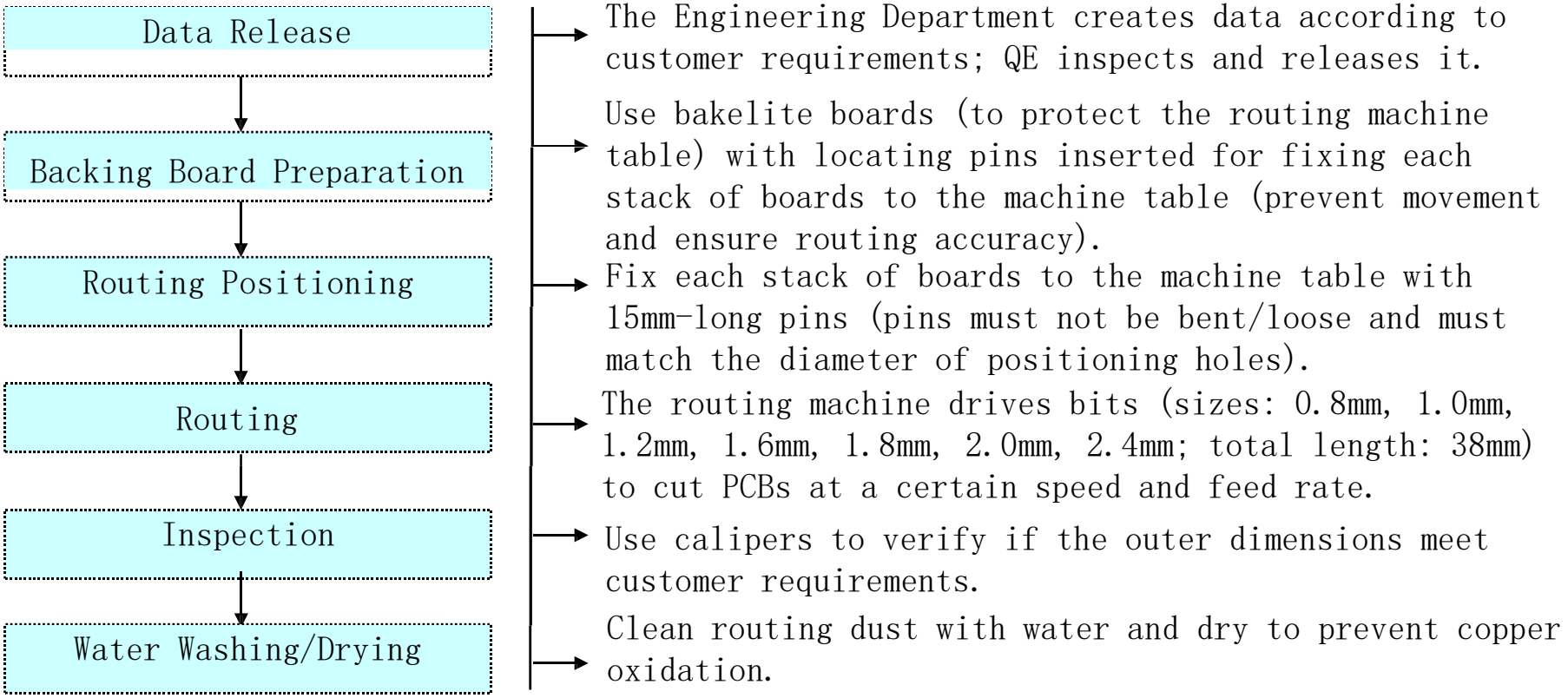
Punching: Use presses and molds to shear PCBs to the required shape.

V-Grooving: Use V-shaped tools to cut "V-grooves" on PCBs for easy board separation after component mounting.

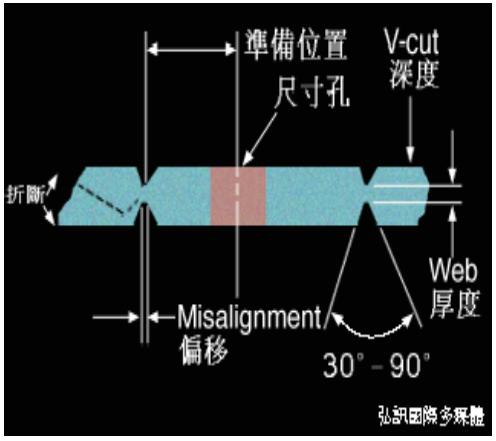
Beveling: Use bevel bits or special tools to cut inclined surfaces at specific angles and depths on PCB edges or inner slots (mainly for gold fingers to facilitate insertion).

12.1 Routing Flow

Use high-speed rotating routing bits to cut PCBs to the required shape.



V-CUT

Process	Purpose	Diagram	Equipment
V－CUT	Cut V-grooves between board units to facilitate separation after customer component soldering.		

Beveling

Process: The beveling machine drives bevel bits (sizes: 3mm, 4mm, 6mm; length: 45mm) to cut PCBs at a fixed speed.

Requirements: Bevel bits must have sufficient rigidity, hardness, and wear resistance.

13. Testing

Process	Purpose	Principle	Notes
Electrical Testing	Simulate board operation, conduct electrical performance tests to detect open/short circuits.	Based on design principles, energize each electrical performance point to test for defects.	Missing tests, board surface damage caused by test machine pressure.

Flying Probe Testing

Process	Flow Introduction	Advantages	Disadvantages	Equipment
Flying Probe Testing	Uses two movable probes (X/Y/Z axes) to test each end of the circuit one by one without expensive fixtures.	1.Suitable for testing ultra-high-density boards. 2.No fixtures required—ideal for samples and small-batch production.	1.Expensive equipment. 2. Slow production speed.	

14. Final Inspection

Flow	Purpose	Inspection Items	
		Dimension	Surface Inspection
Final Inspection	Conduct final quality verification of finished products during the manufacturing process.	1. Outer dimension 2. Hole-to-edge distance 3. Board thickness 4. Hole diameter 5. Annular ring size	1. Hole voids 2. Hole plugging 3. Exposed copper 4. Foreign matter 5. Extra/missing holes 6. Gold finger defects 7. Legend defects

15. Packaging

Process	Purpose	Principle	Flow Introduction	Notes
Packaging	Package boards into boxes for easy transportation	Use a vacuum packaging machine to seal boards	Count Quantity → Vacuum Sealing → Carton Packaging	Board damage, scratc hes

15. Packaging

Packaging provides protection, identification, and aesthetics for products.

1. Humidity Indicator Card
2. Inner Label
3. Outer Label
4. Barcode
5. Desiccant
6. RoHS Compliance Label
7. HF (Halogen-Free) Label

Hand in Hand Toward a Shared and Glorious Future

Thank You!